

ASUS CONFIDENTIAL

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MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

Lanai Discrete VGA nVidia NB8M Schematics Document

uFCPGA Mobile Merom
Intel Crestline-PM + ICH8M

2007-03-19

REV : 1.2(DELL: X02)

MB PCB

Part Number	Description
DAB0000480L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???

PCB P/N: ???

<Variant Name>

PROJECT: **Lanai**

REVISION
1.2

DATE: *Monday, March 19, 2007*
SHEET **1** OF **69**

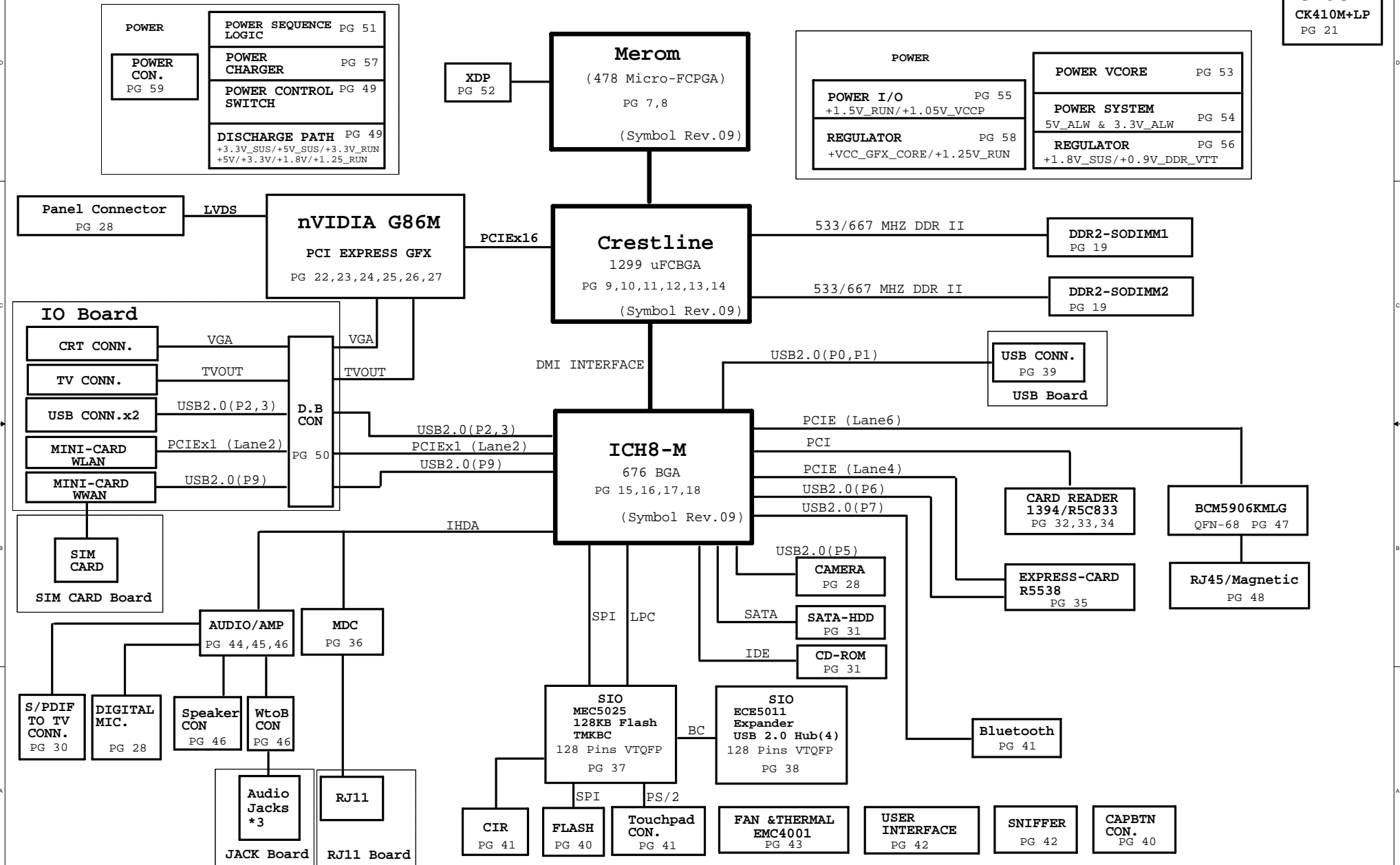
DESCRIPTION: *Cover Page*

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Terry Lin

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LANAI: DISCRETE



<Variant Name>

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DESCRIPTION:
BLOCK DIAGRAM

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
STANLY HSU

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01	Cover Page	
02	Schematic Block Diagram	
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05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU (Merom 、 Penryn)	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM(533MHz 、 667MHz)	
21	Clock Generator (CK410M+LP)	
22-27	VGA (nVIADA - G86M & GDDR3)	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 (R5C833)	
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36	MDC CONN	
37	EC (MEC5025)	
38	SIO (ECE5011)	
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40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
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47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
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53-59	Power Circuit	
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Pg#	Description	DNI LIST
64	Power circuit Change list	
R01	Modem board cover page	
R02	RJ-11 CONN	
R03	Modem board Change list	
U01	USB board cover page	
U02	USB PORT (SINGLE * 2)	

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DESCRIPTION: INDEX

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Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN

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DESCRIPTION:

Bus Connection

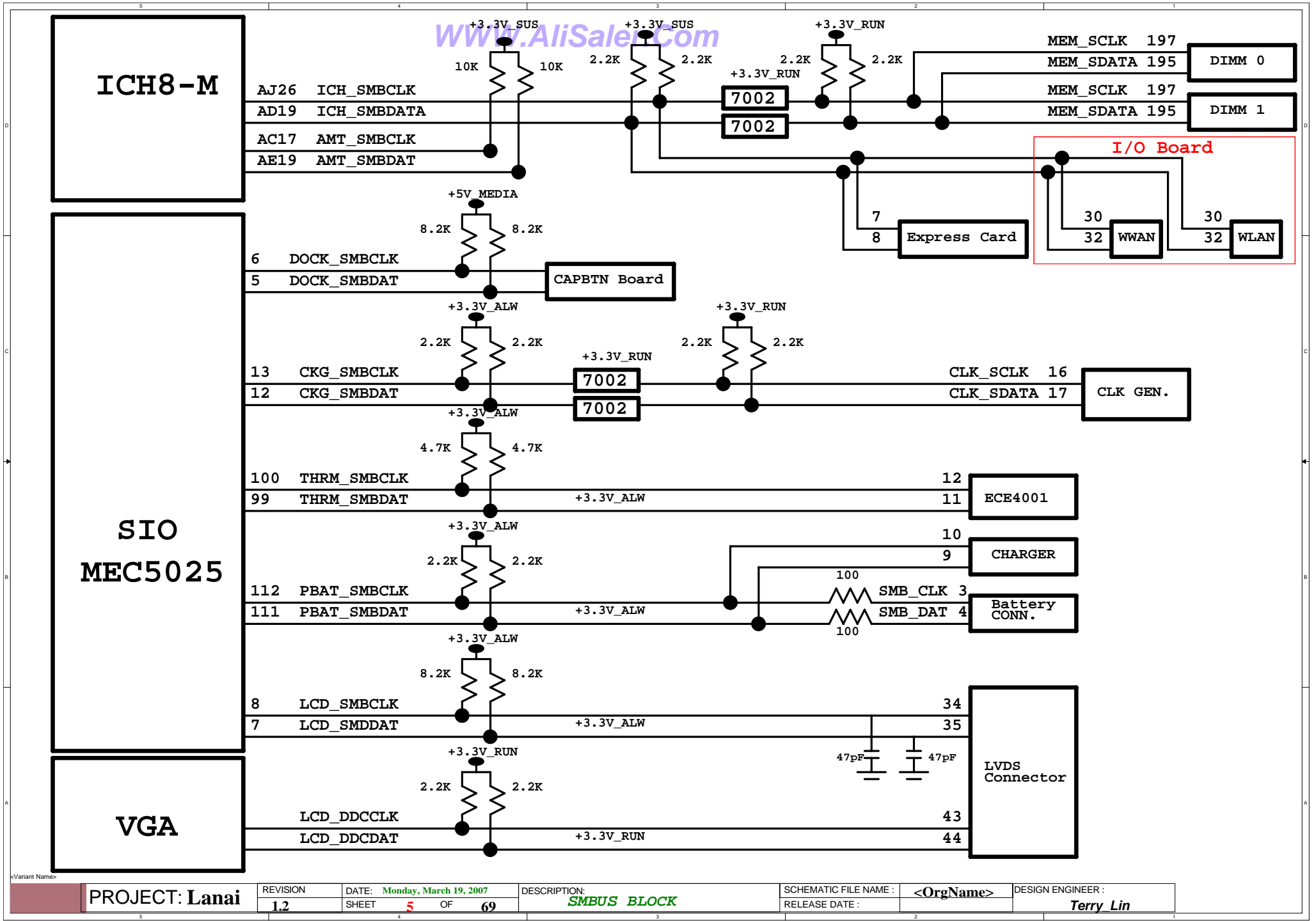
SCHEMATIC FILE NAME :

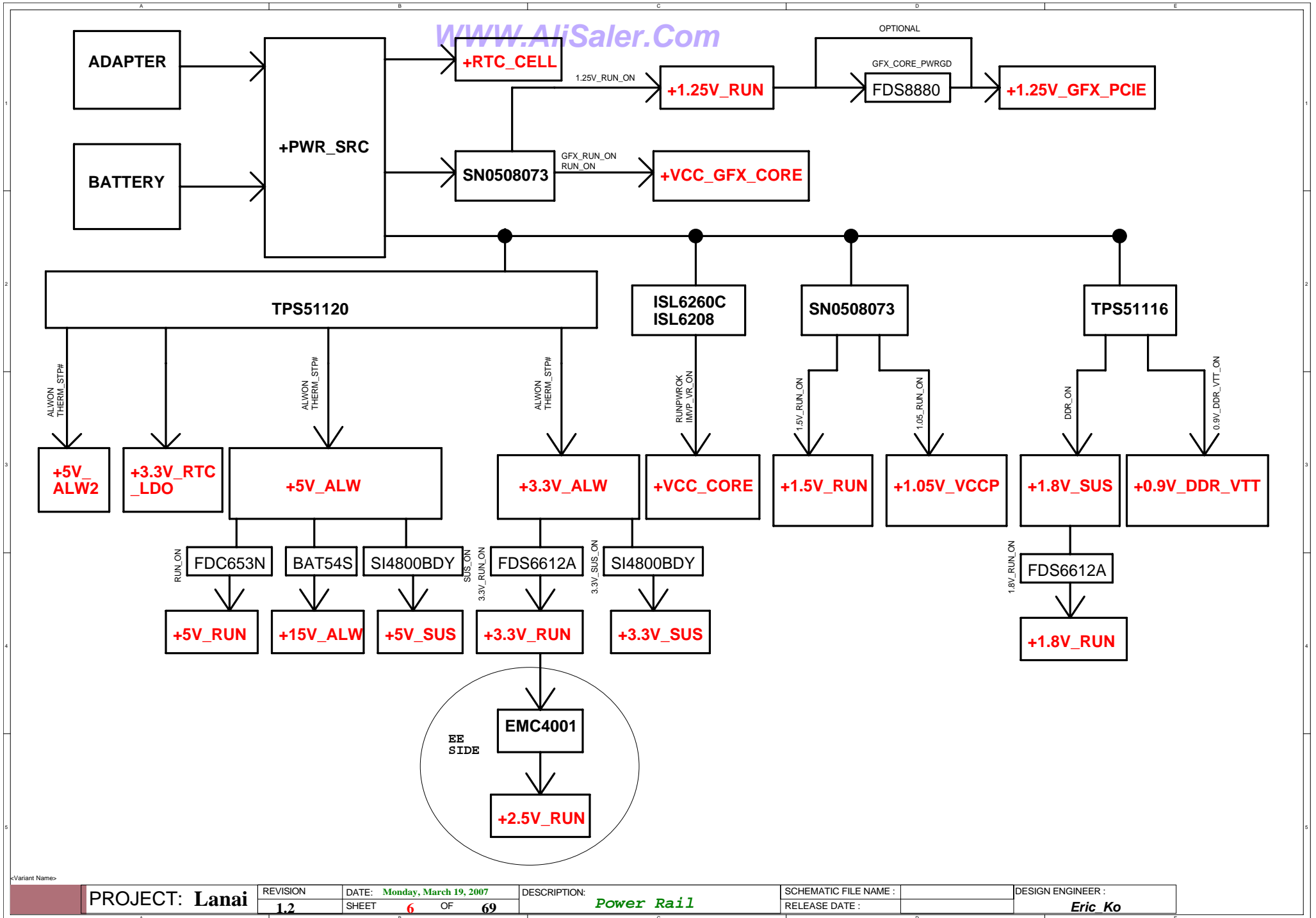
<OrgName>

RELEASE DATE :

DESIGN ENGINEER :

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<Variant Name>

PROJECT: **Lanai**

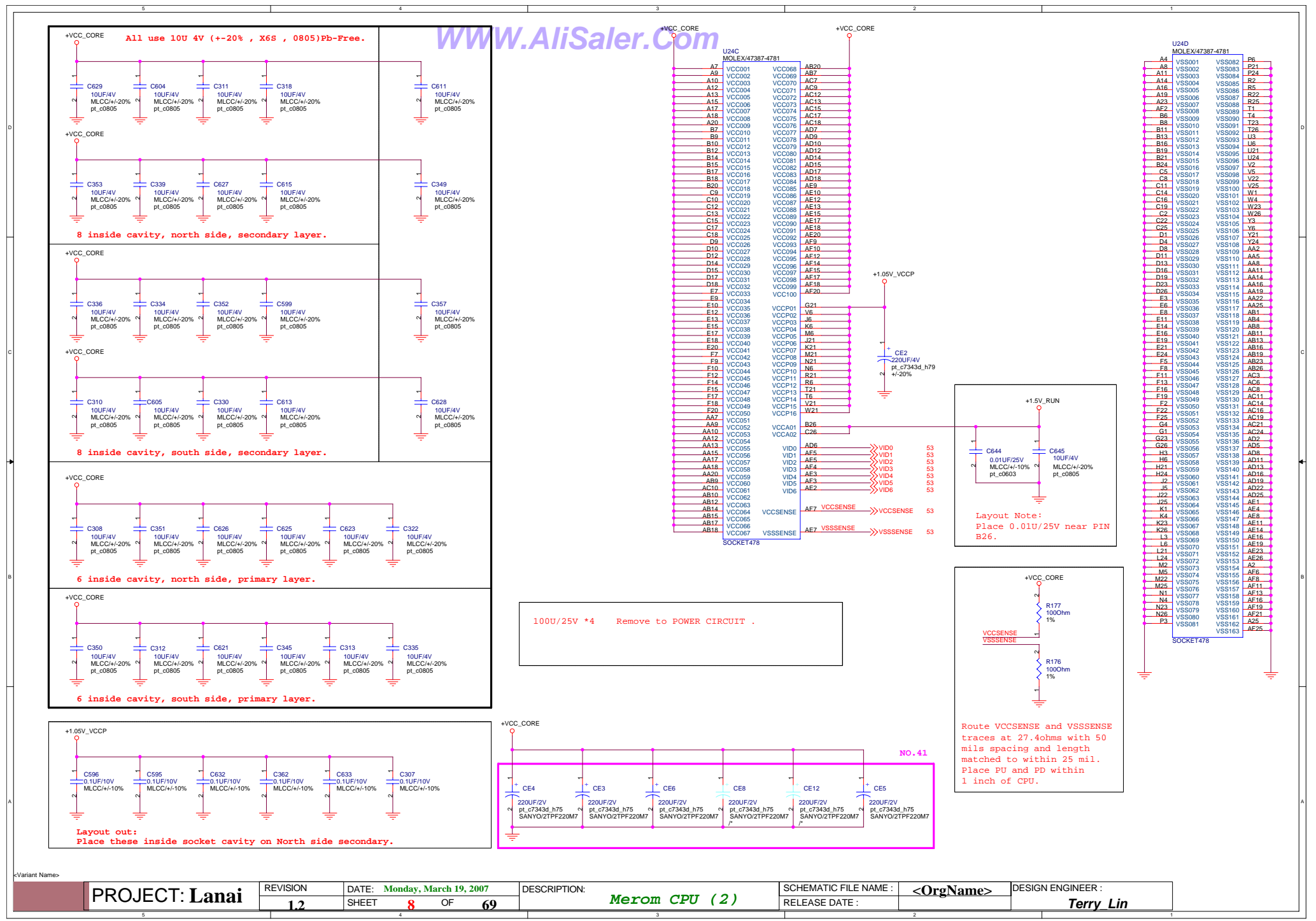
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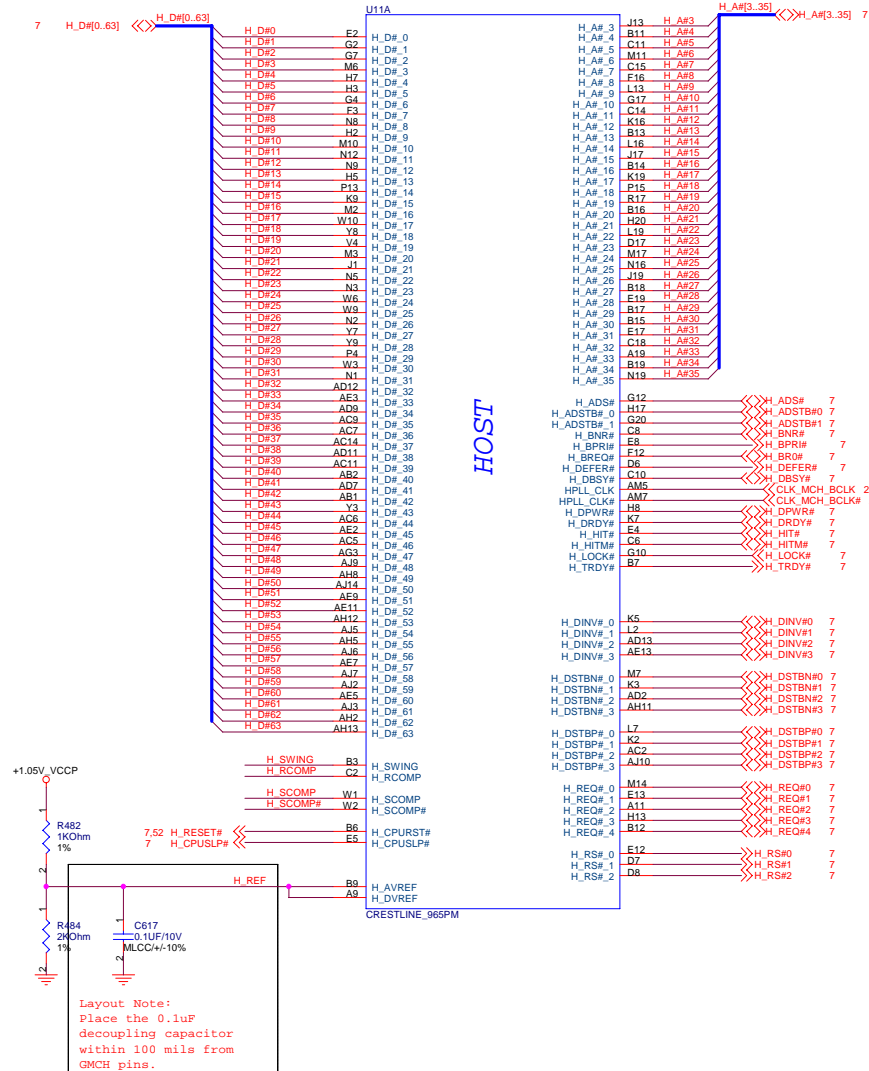
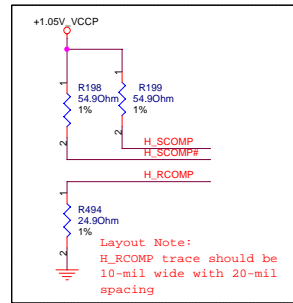
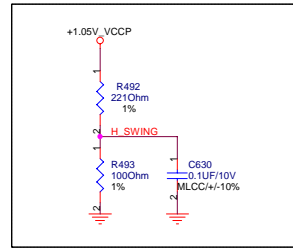
DATE: **Monday, March 19, 2007**
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DESCRIPTION: **Power Rail**

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Eric Ko





<Variant Name>

PROJECT: Lanai

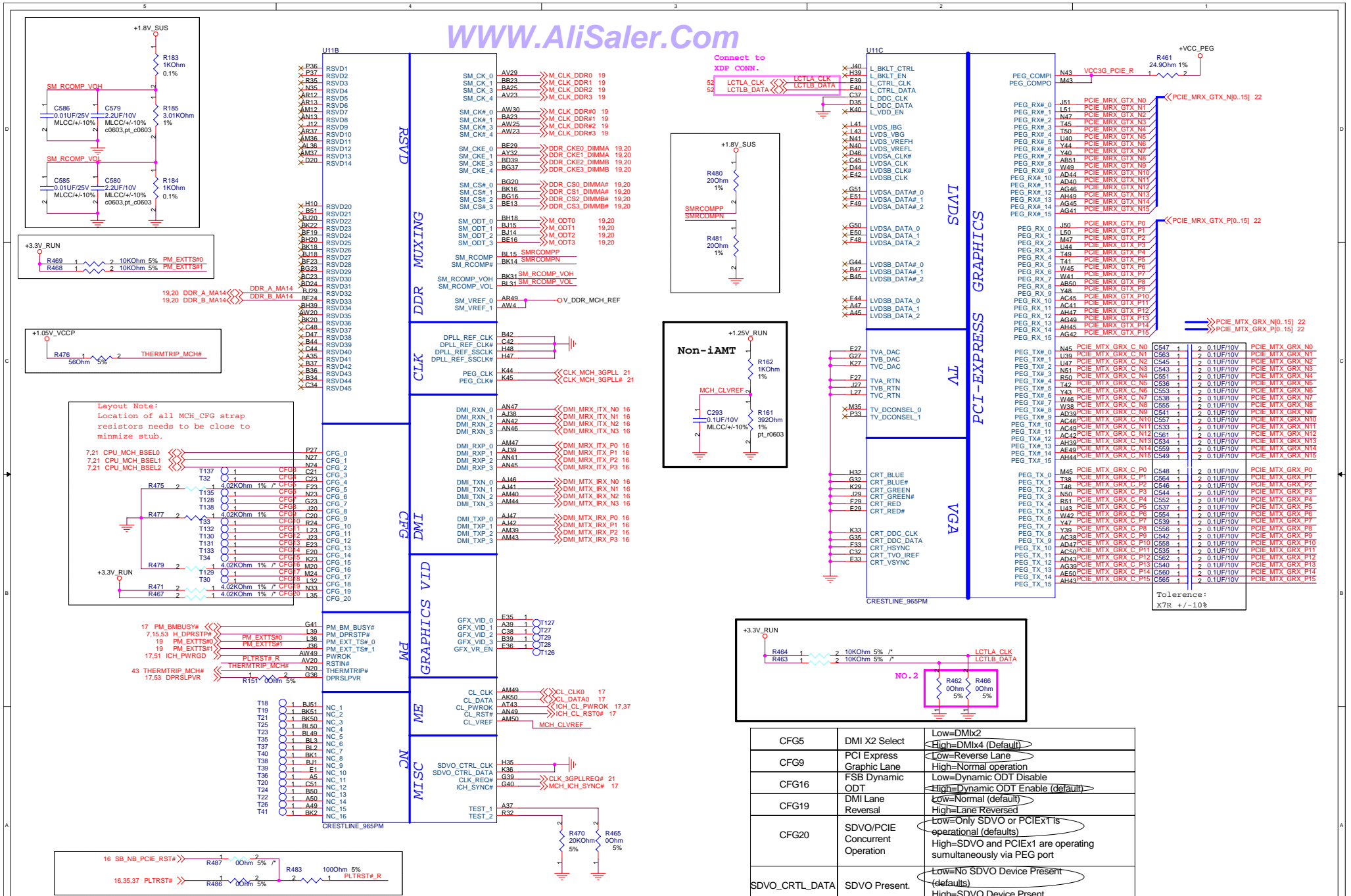
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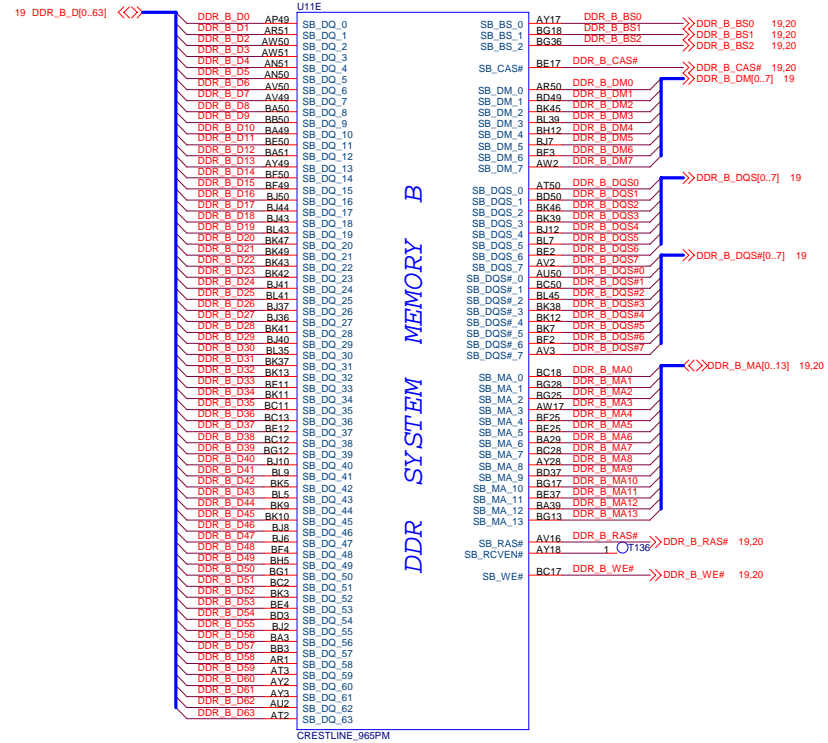
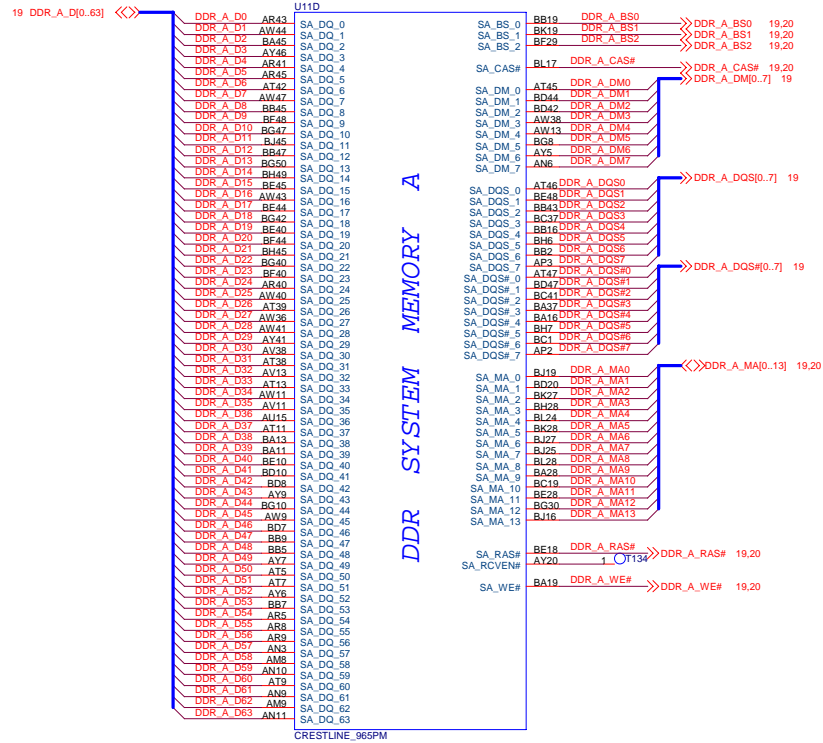
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DESCRIPTION: Crestline(HOST)

SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER: Ivan Chou





<<Variant Name>

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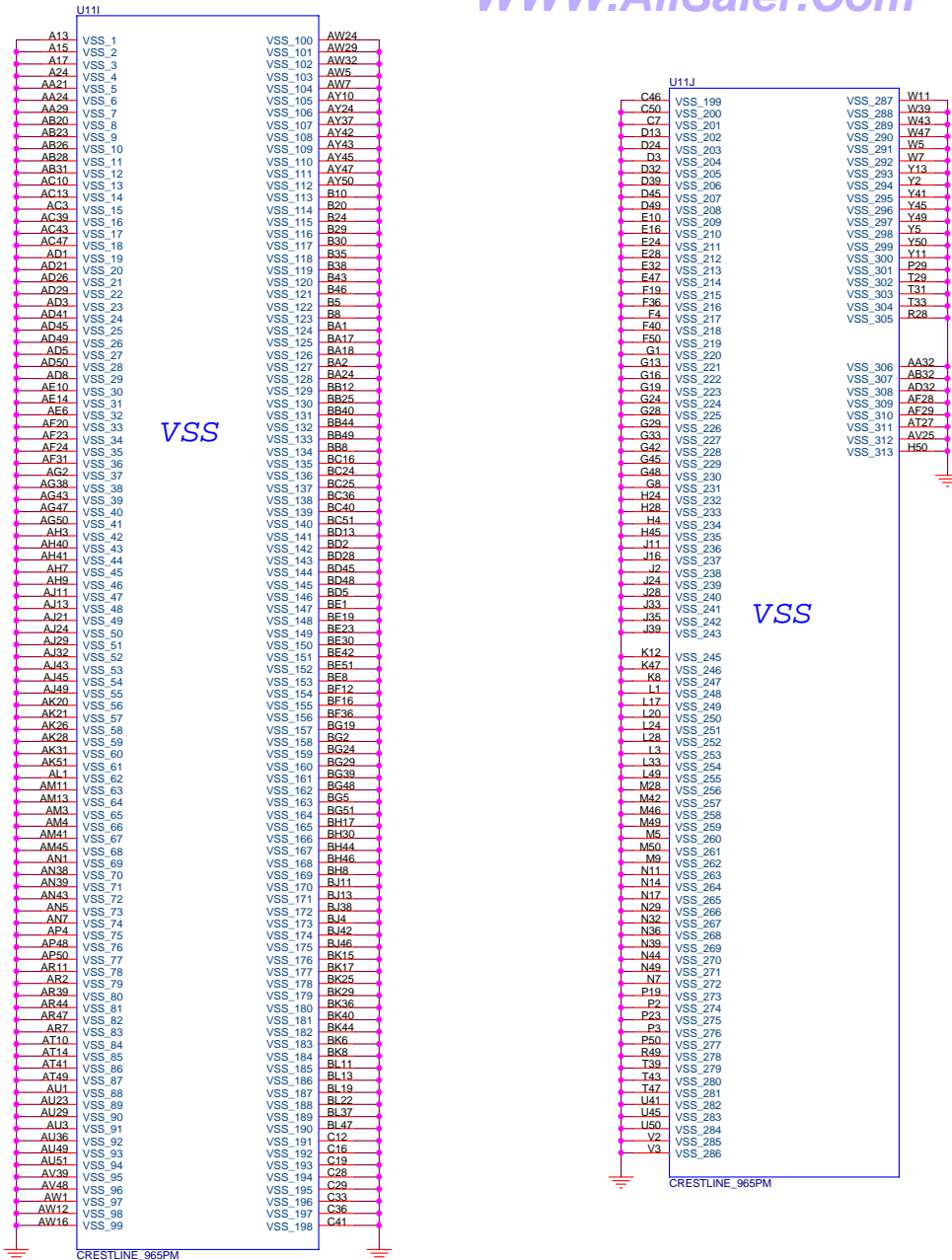
DESCRIPTION: Crestline(DDR2)

SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER: Ivan Chou







<Variant Name>

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DESCRIPTION:

Crestline(VSS)

SCHEMATIC FILE NAME :

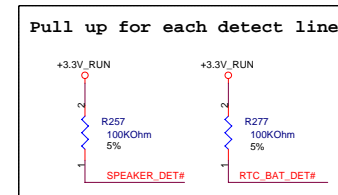
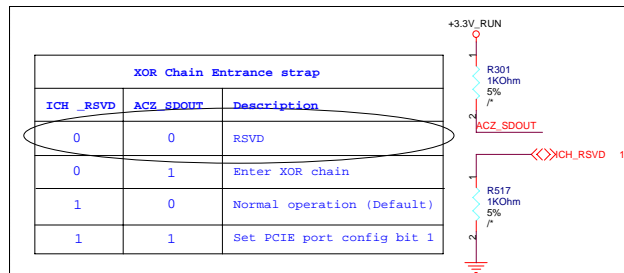
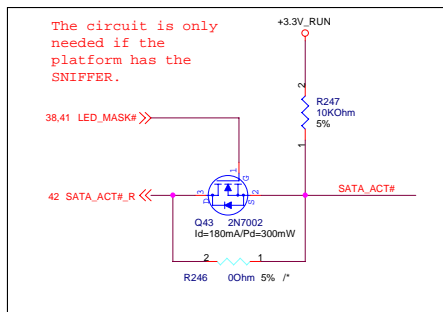
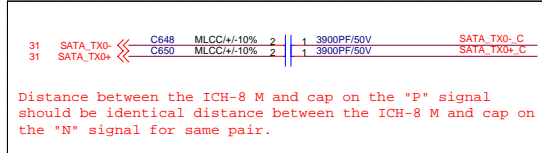
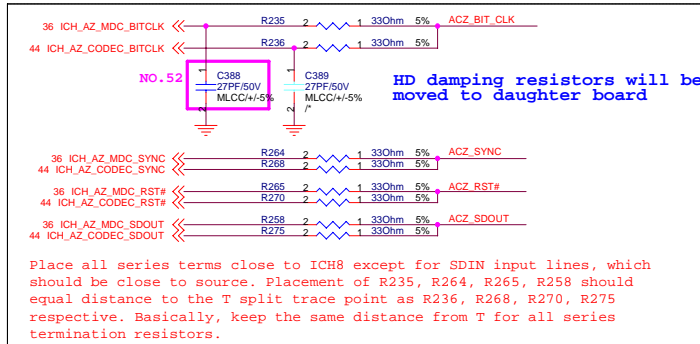
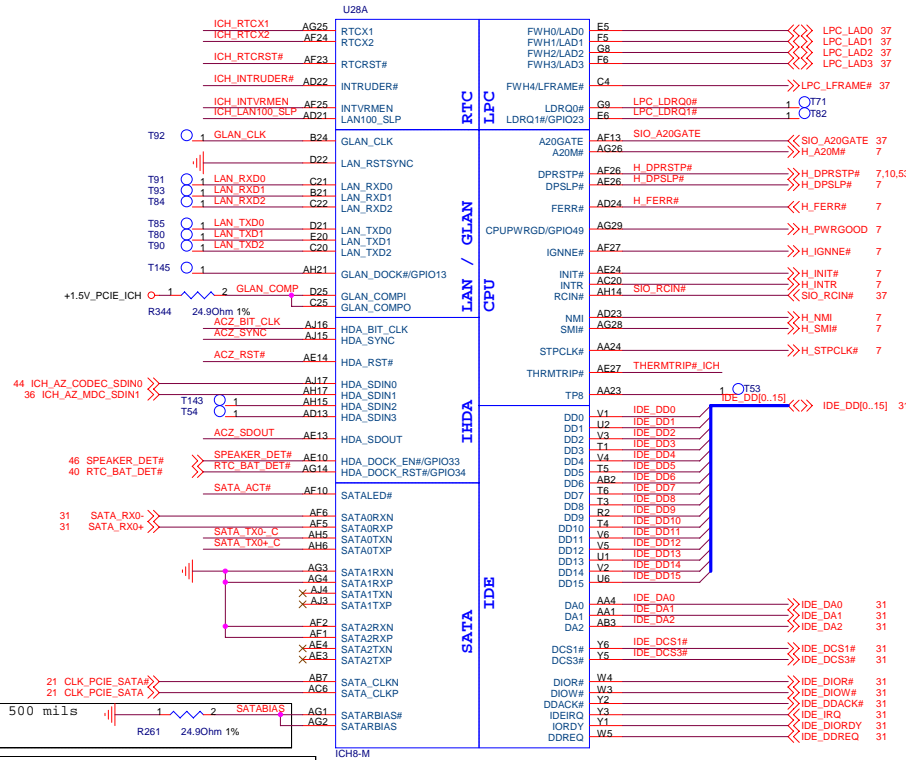
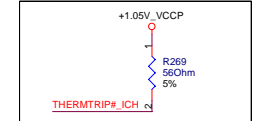
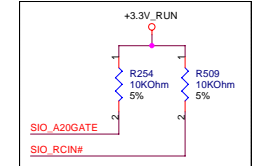
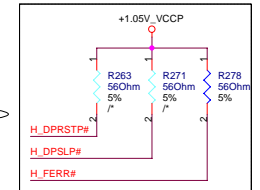
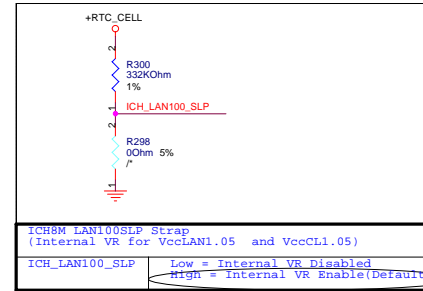
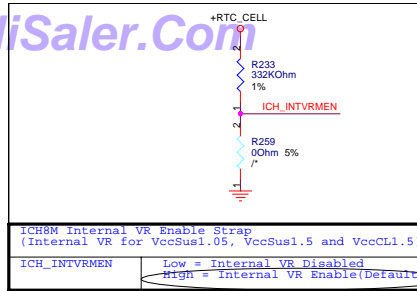
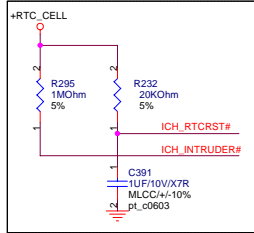
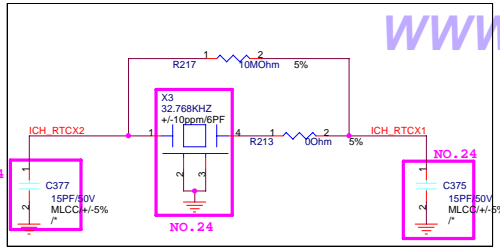
<OrgName>

DESIGN ENGINEER :

Ivan Chou

RELEASE DATE :

NO.24



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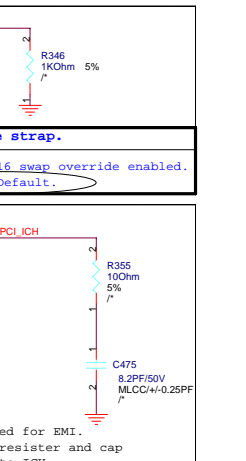
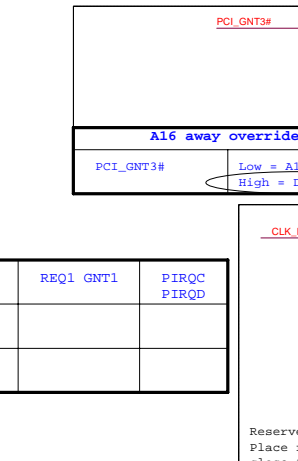
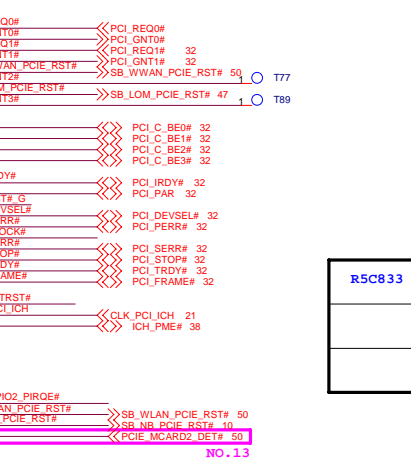
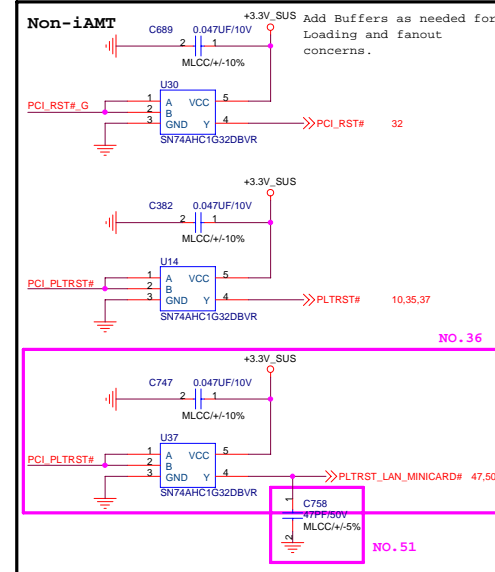
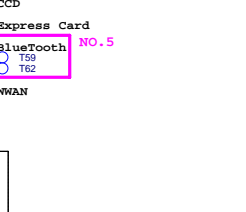
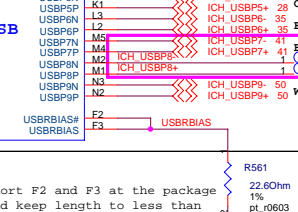
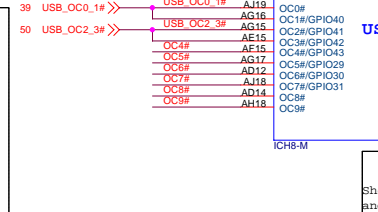
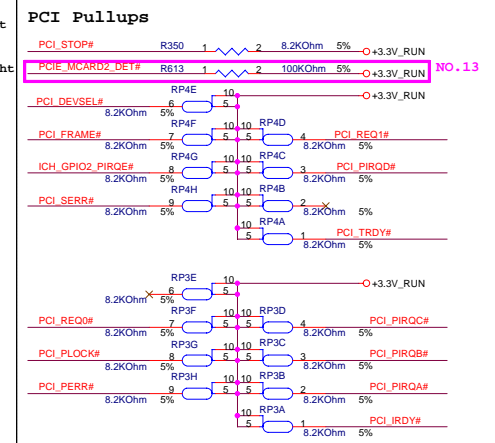
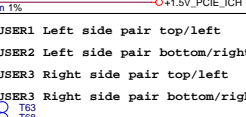
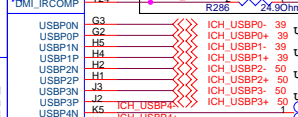
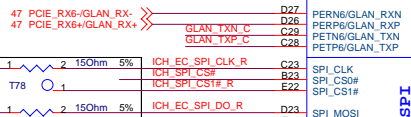
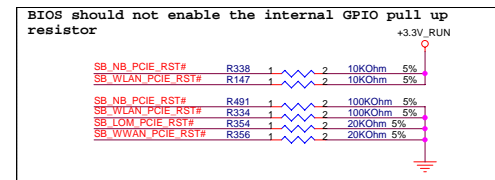
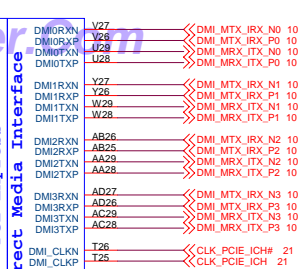
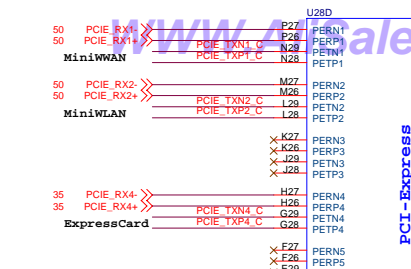
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DESCRIPTION:
ICH8: IDE/AC97/LPC/RTC

SCHEMATIC FILE NAME:
RELEASE DATE:

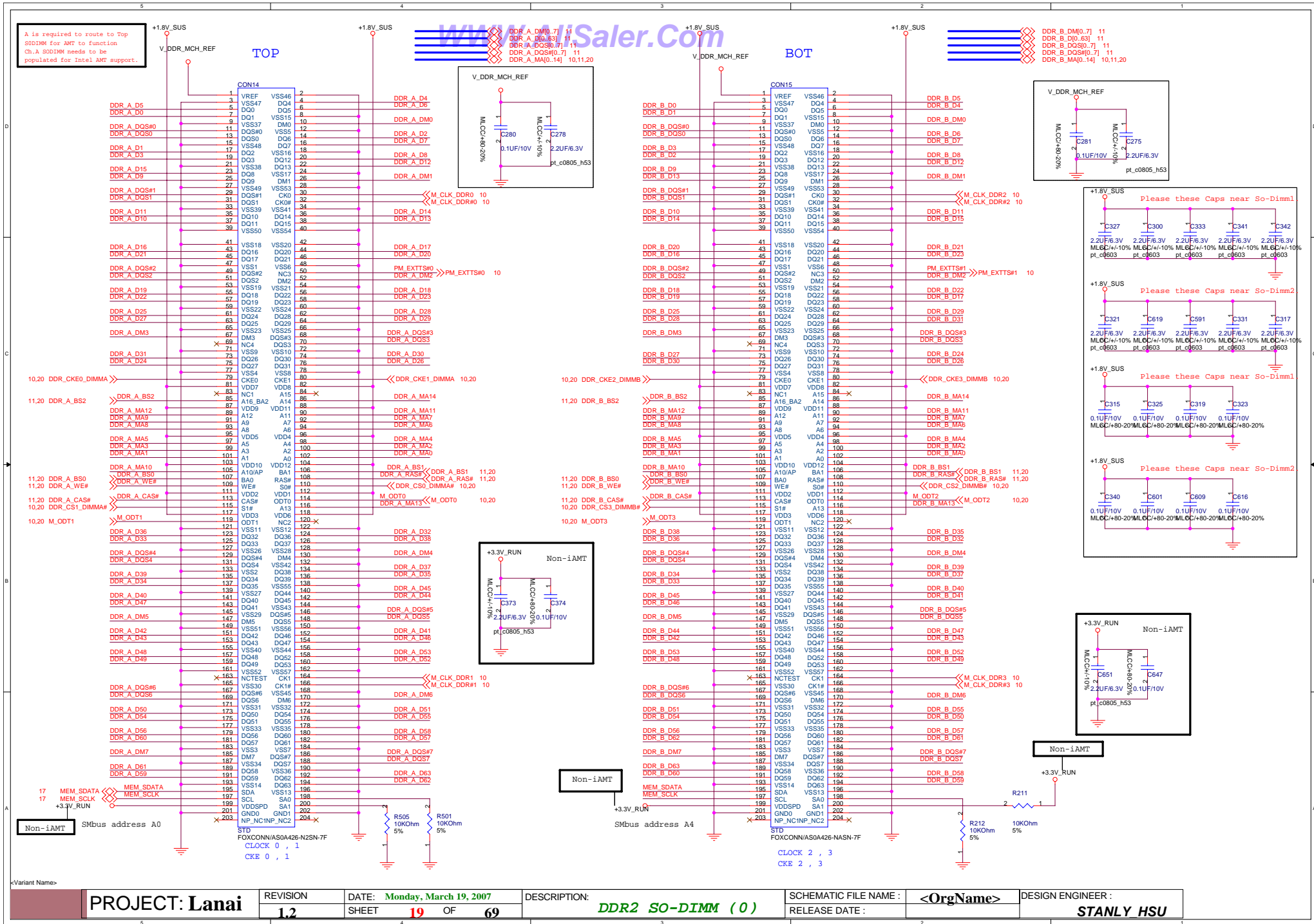
<OrgName>

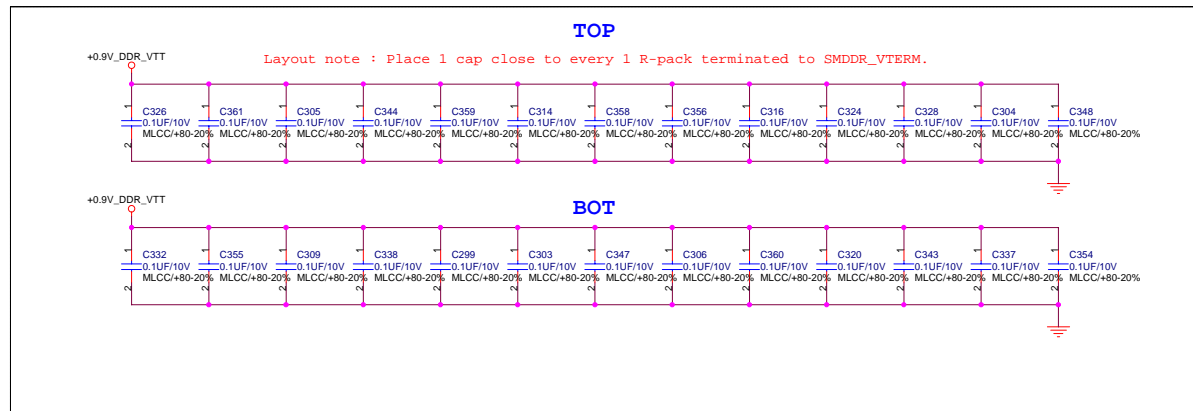
DESIGN ENGINEER:
Terry Lin



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 16 OF 69	ICH8 : PCI/INT/DMI/USB	RELEASE DATE :	Terry Lin

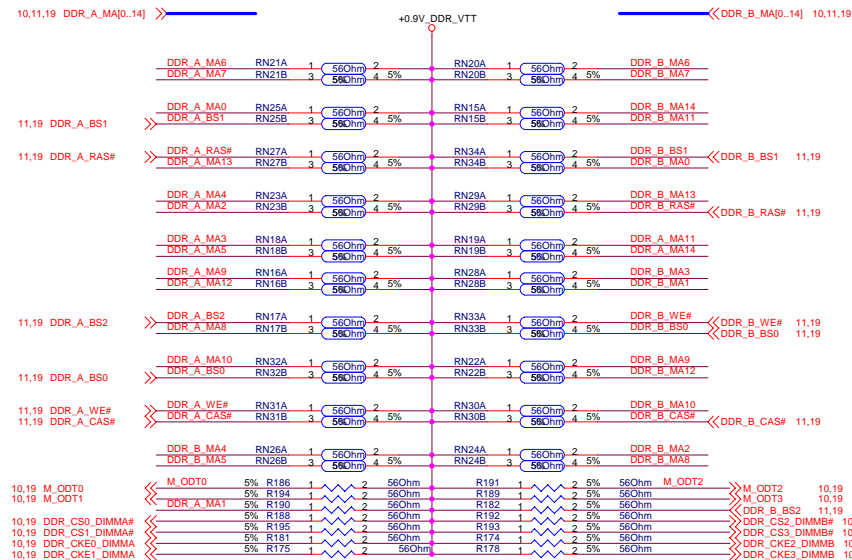






Please these resistor
closely DIMMA, all
trace length<750 mil.

Please these resistor
closely DIMMB, all
trace length<750 mil.



<Variant Name>

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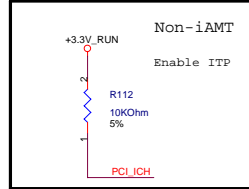
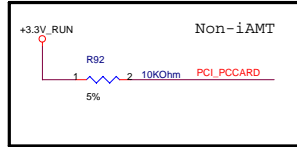
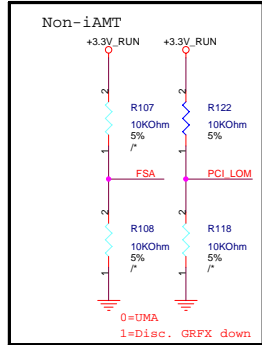
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DESCRIPTION: **DDR2 SO-DIMM (1)**

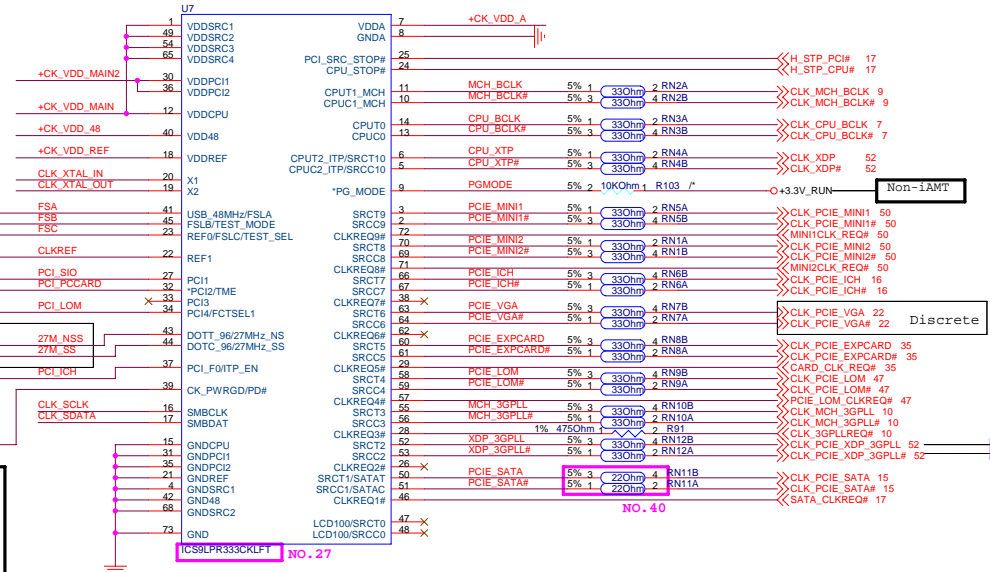
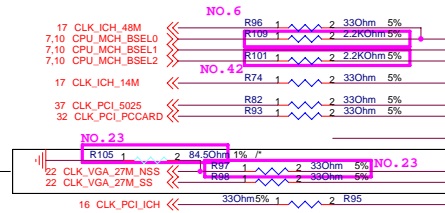
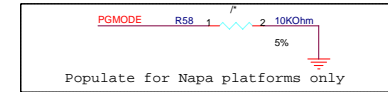
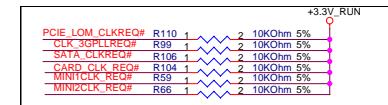
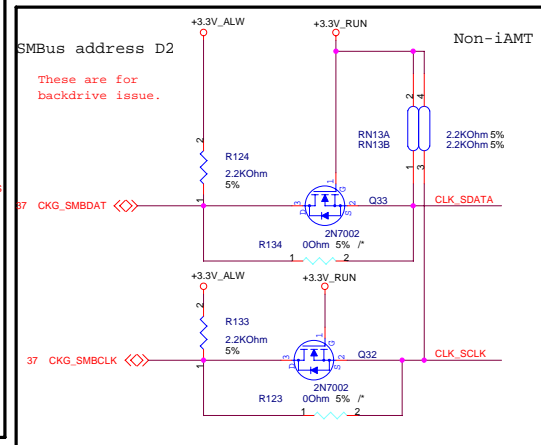
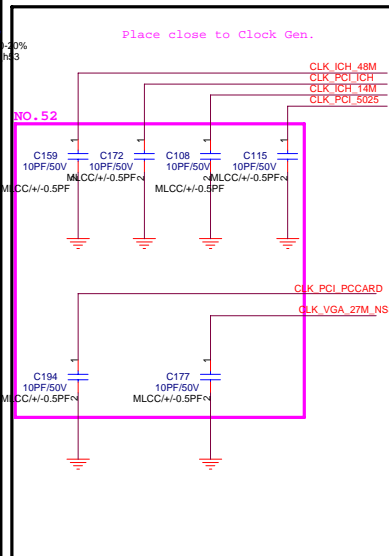
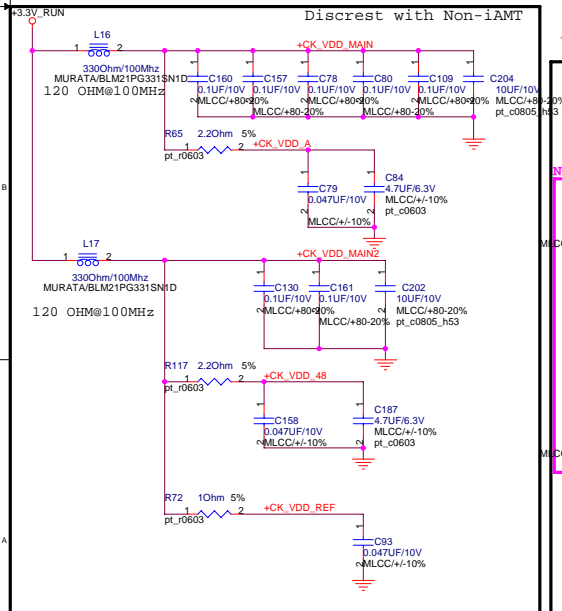
SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :
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CLK_VGA_27M_NSS (VGA XTALIN) OPTION	G7X	NB8X
R97	147ohm	33 ohm
R105	84.5 ohm	no-stuf
clk. voltage	1.2V	3.3V



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

FCTSEL1 (PIN 34)	Pin43	Pin44	Pin47	Pin48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc.	27Mout	27M_SSout	SRCT0	SRCC0
GRFX down				

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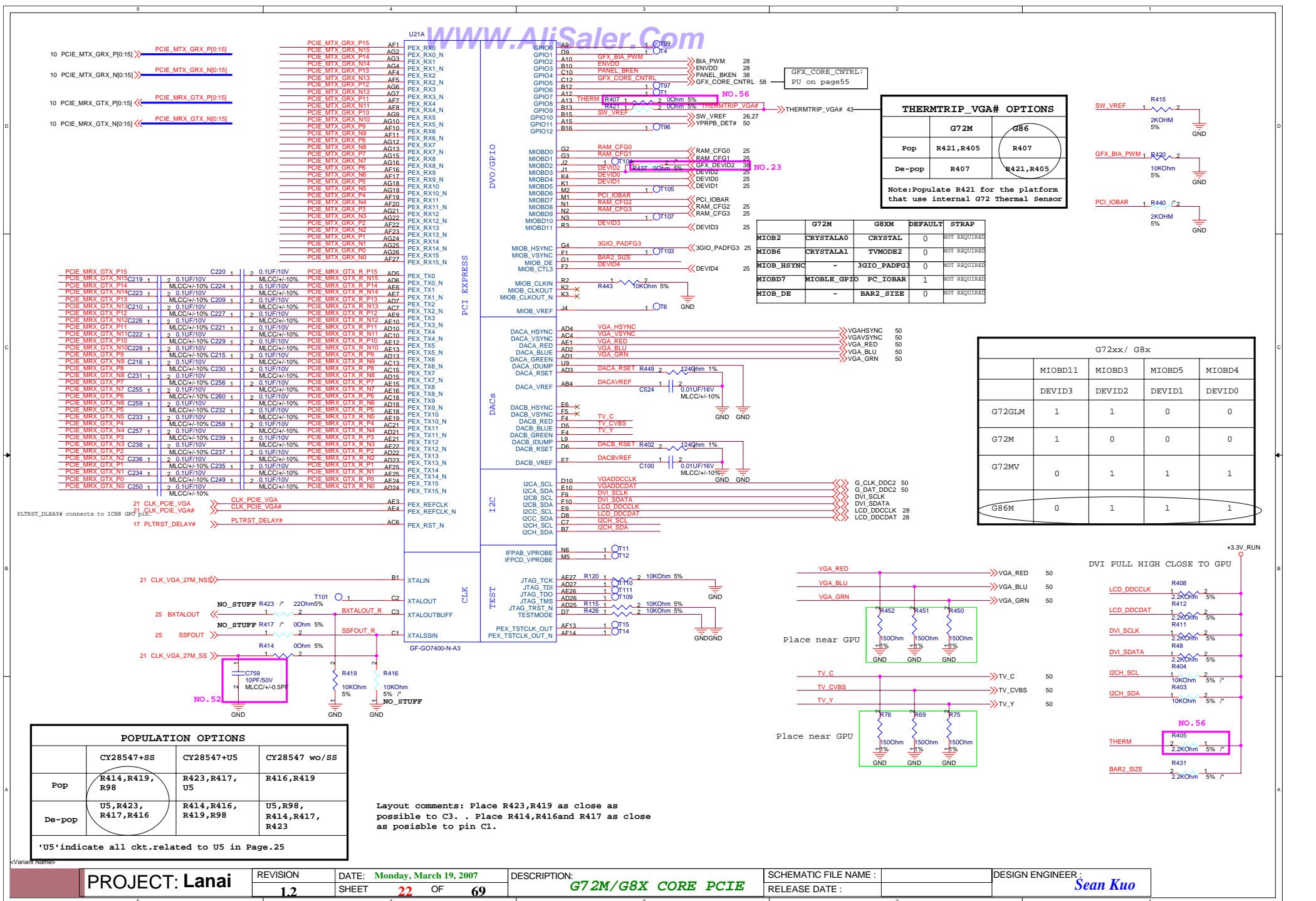
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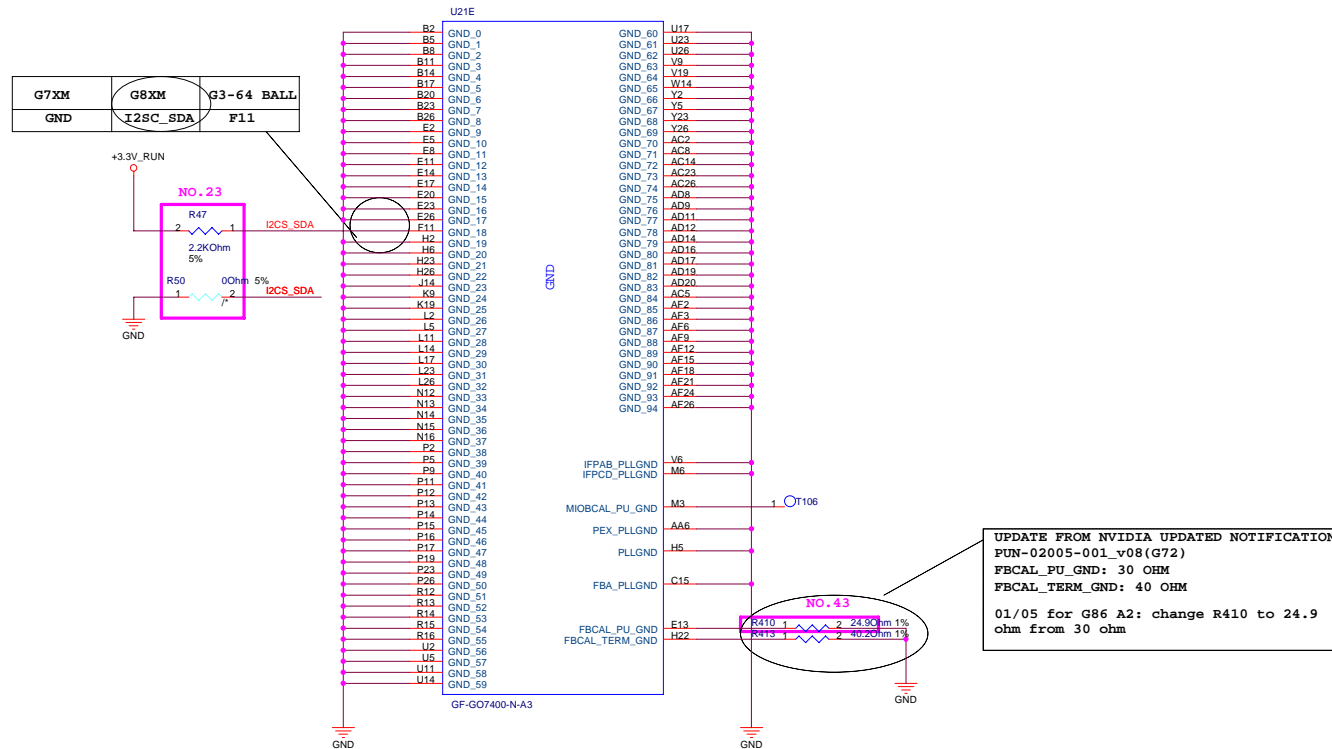
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DESCRIPTION: CLK GEN. CY28547

SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER:
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<Variant Name>

PROJECT: Lanai

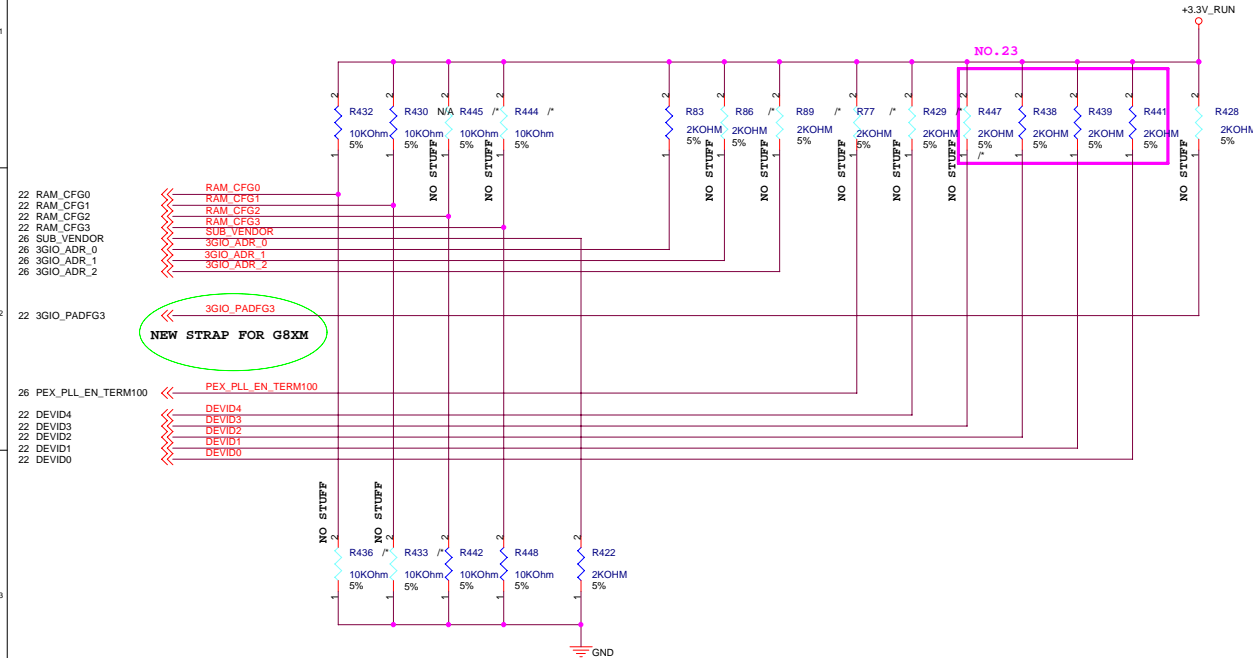
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DATE: Monday, March 19, 2007
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DESCRIPTION:
G7XM/G8X CORE GND

SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER:
Sean Kuo



STRAPS	PIN	DESCRIPTION	Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT,Serial SST45VF=10, LPC=11	01
SUB_VENDOR	MIOAD1		0
PEX_PLL_TERM	MIOAD0		0
RAM_CFG[3:0]	FOR GDDR1	8Mx32 DDR monolithic (32bit) 300MHz, 1.8V	1001
		4Mx32 DDR generic (64bit) 1.8V I/O	0100
		4Mx32 DDR generic (32bit) 1.8V I/O	1100
	FOR GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
		Hynix 8Mx32 500MHz, 1.8V	0111
		Samsung 8Mx32 500MHz, 1.8V	0110
		Infineon 16Mx32 GDDR3 ,1.8V	0001
		Hynix 16Mx32 GDDR3 1.8V	0010
		Samsung 16Mx32 GDDR3 1.8V	0011

Internal Pull-down

MIOAD0, MIOAD6,

MIOAD8, MIOAD9

MIOAD1----SUB_VENDOR

MIOAD0----PEX_PLL_EN_TERM

MIOAD6----3GIO_ADR_0

MIOAD8----3GIO_ADR_1

MIOAD9----3GIO_ADR_2

0, SYSTEM BIOS

[2:0] 001 for NV43/NV44

010 for G7x, NV42

MIOBD4----PCI_DEVID0

MIOBD5----PCI_DEVID1

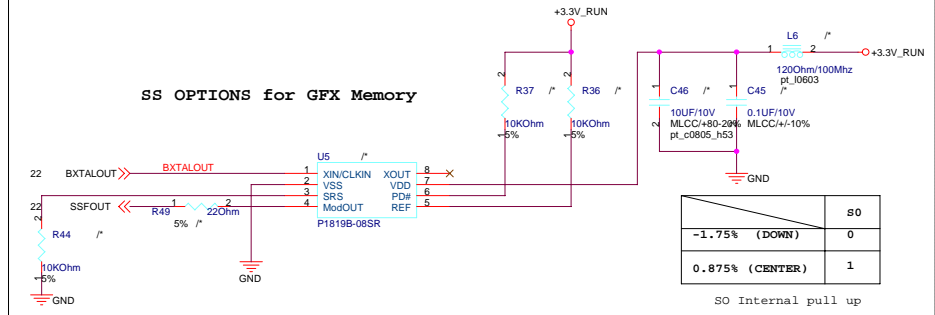
MIOBD3----PCI_DEVID2

MIOBD11----PCI_DEVID3

1000, G72M

0111, G72MV

SS OPTIONS for GFX Memory



M08 HAS REMOVED THIS PORTION
INSTALL OR NOT?

<Variant Name>

PROJECT: Lanai

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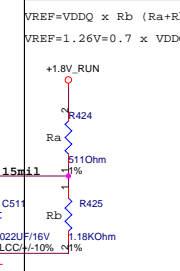
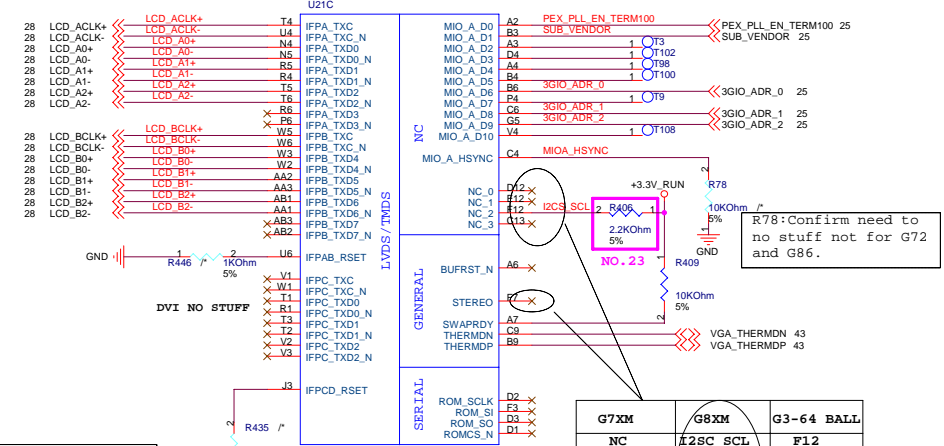
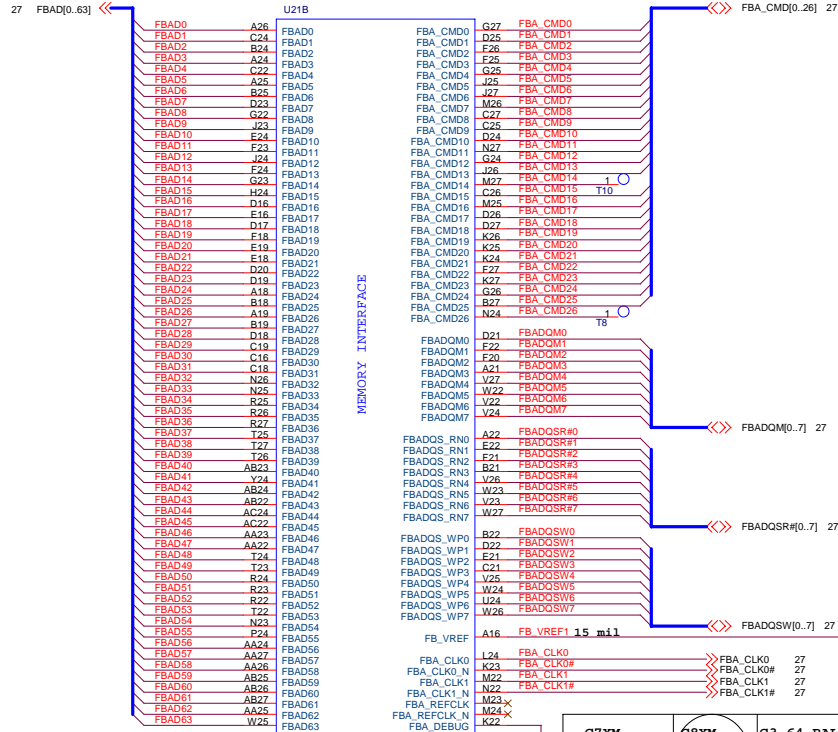
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DESCRIPTION:
G72M/G8X STRAPPING PAGE

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DESIGN ENGINEER:
Sean Kuo



G7XM	G8XM	G3-64 BALL
NC	I2SC_SCL	F12
STEREO	DACB_CS	F7
NC	GPIO13	C13
NC	GPIO14	E12

R78: Confirm need to no stuff not for G72 and G86.

<Variant Name>

PROJECT: Lanai

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DESCRIPTION: G72M/G8X FBA/LVDS

SCHEMATIC FILE NAME:
RELEASE DATE:

DESIGN ENGINEER: Sean Kuo



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D							D
C							C
B							B
A							A
<Variant Name>	PROJECT: Lanai		REVISION 1.2	DATE: Monday, March 19, 2007 SHEET 29 OF 69	DESCRIPTION: VGA CRT CON	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Sean Kuo



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	3
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RELEASE DATE :

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	Se
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14/14/14/ Al-Solar Com

1

PROJECT: Lanai

REVISION
1.2

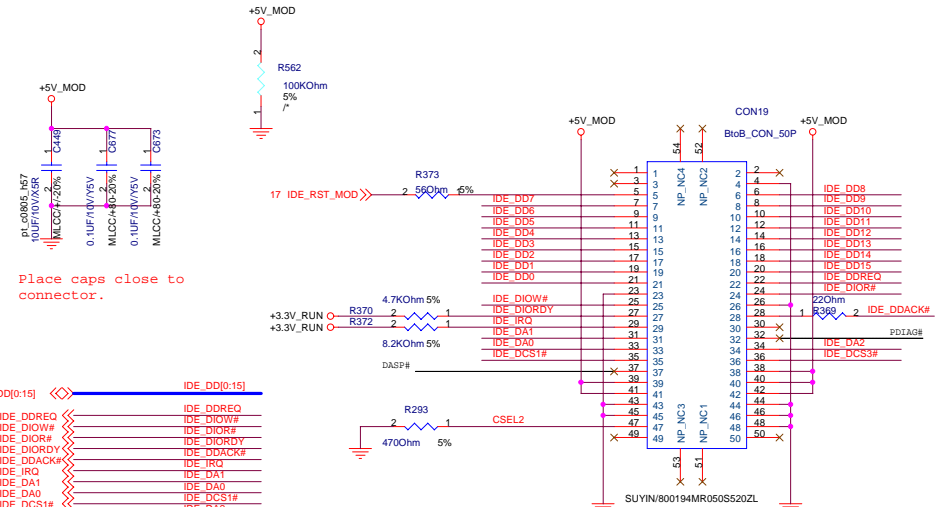
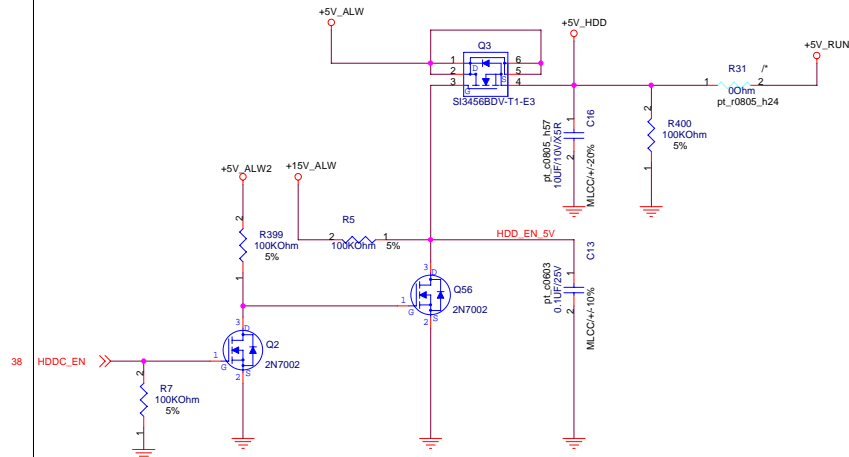
DATE: Monday, March 19, 2007
SHEET 30 OF 69

DESCRIPTION:	TV OUT CON
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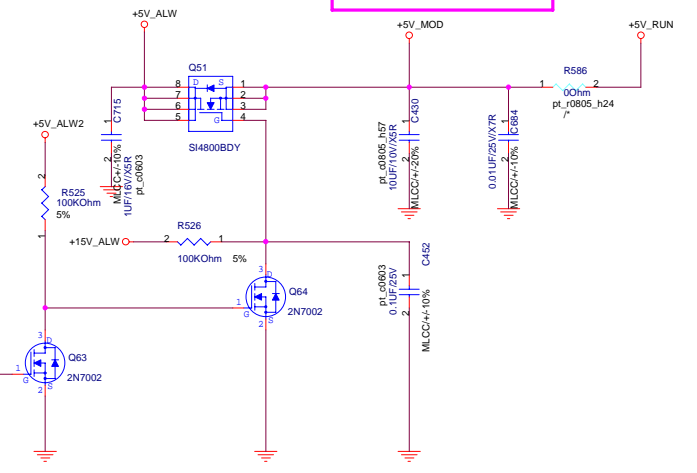
SCHEMATIC FILE NAME :
RELEASE DATE :

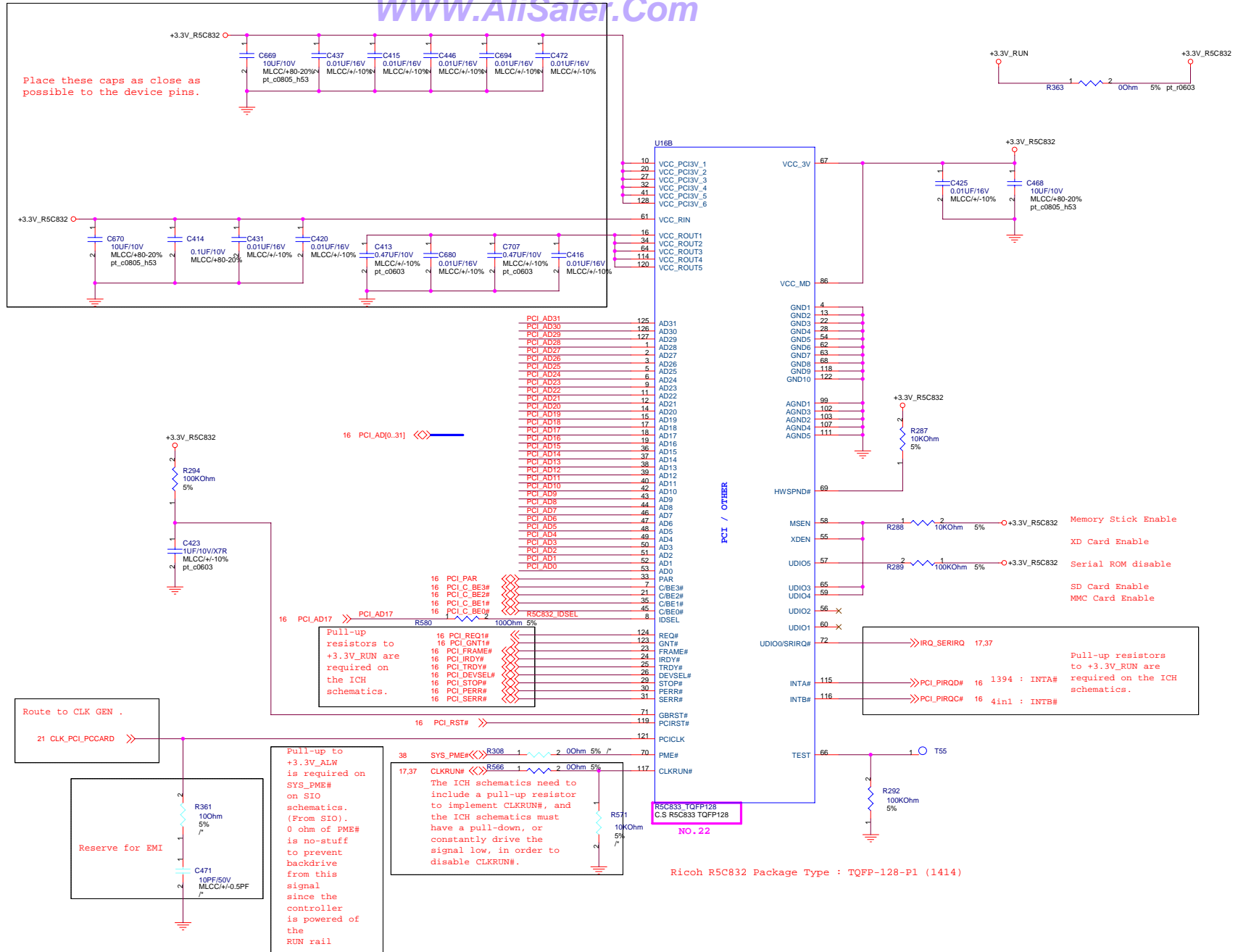
DESIGN ENGINEER :	<i>Sean Kuo</i>
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15	IDE_DD[0:15]	IDE_DD[0:15]
15	IDE_DDREQ	IDE_DDREQ
15	IDE_DIOW#	IDE_DIOW#
15	IDE_DIOR#	IDE_DIOR#
15	IDE_DIORDY	IDE_DIORDY
15	IDE_DIORDY#	IDE_DIORDY#
15	IDE_DBACK#	IDE_DBACK#
15	IDE_IRQ	IDE_IRQ
15	IDE_DA1	IDE_DA1
15	IDE_DA0	IDE_DA0
15	IDE_DCS1#	IDE_DCS1#
15	IDE_DA2	IDE_DA2
15	IDE_DCS3#	IDE_DCS3#



MODPRES# and USB_IDE#
are removed.





<Variant Name>

PROJECT: Lanai

REVISION
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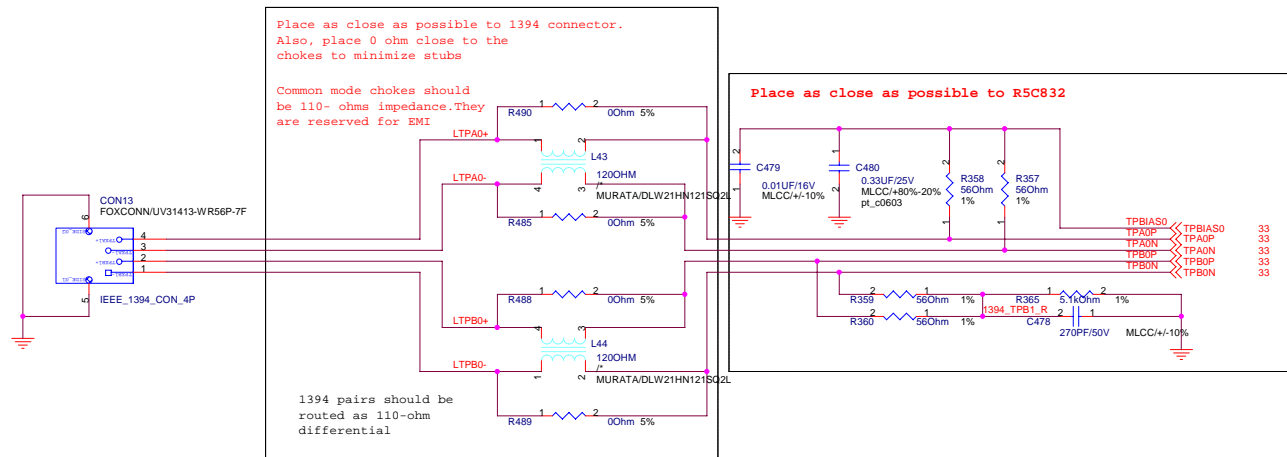
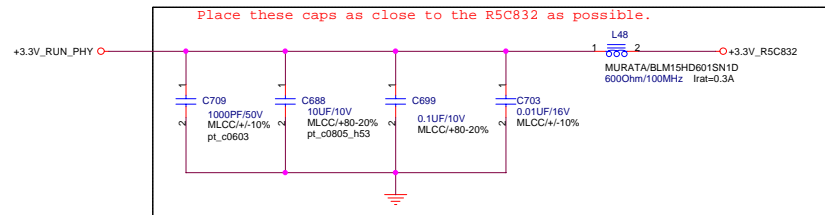
DESCRIPTION:
R5C833 - PCI INTERFACE

SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :
Terry Lin





<Variant Name>

PROJECT: Lanai

REVISION
1.2

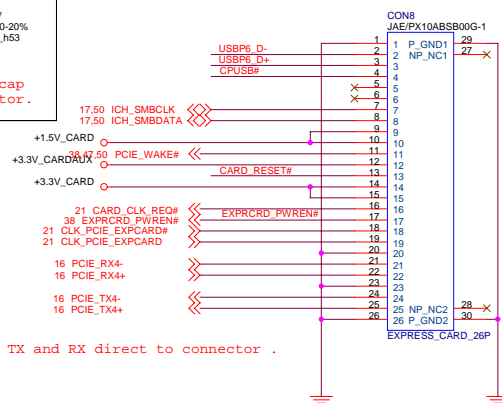
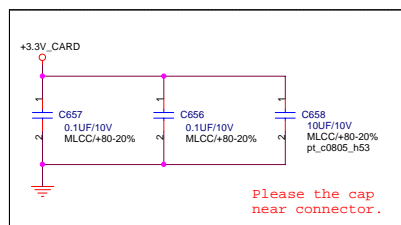
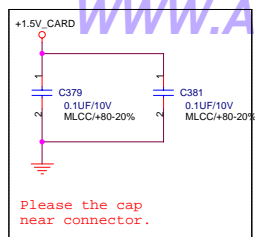
DATE: Monday, March 19, 2007
SHEET 34 OF 69

DESCRIPTION:
R5C833 - IEEE1394 PART

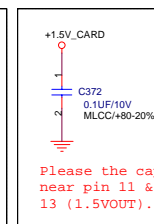
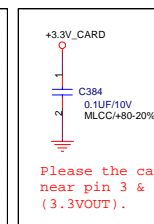
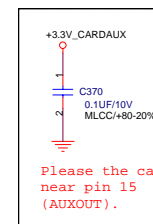
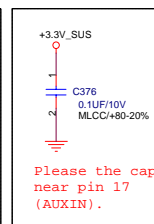
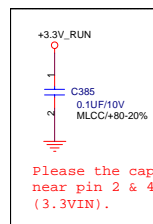
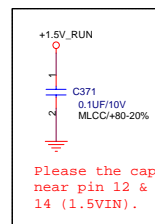
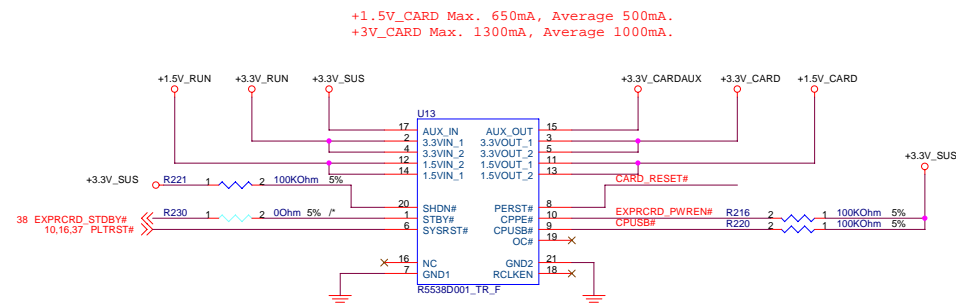
SCHEMATIC FILE NAME :
RELEASE DATE :

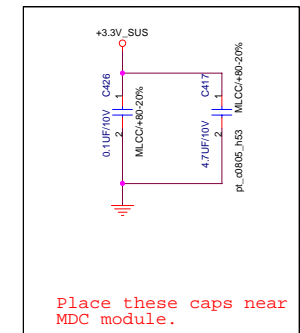
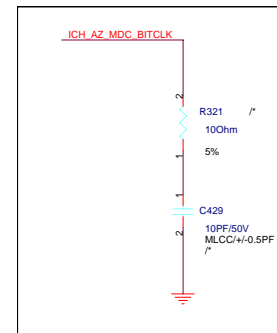
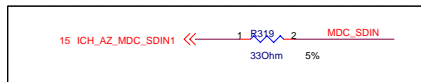
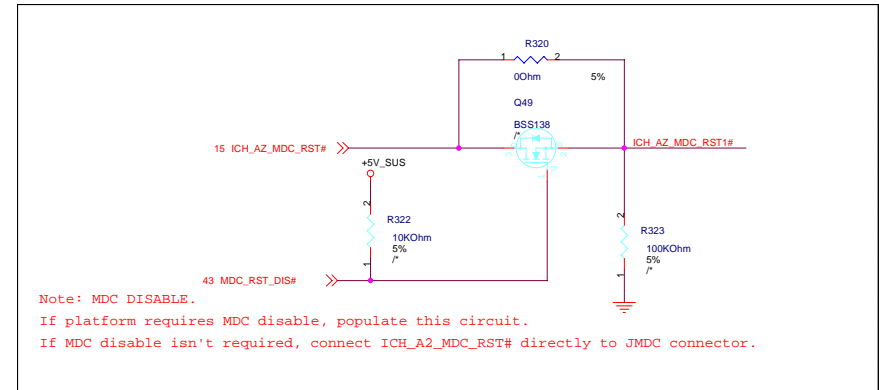
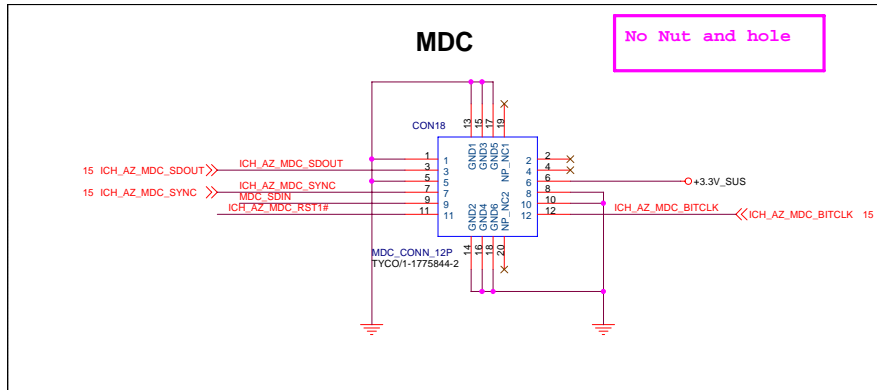
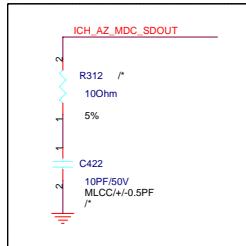
<OrgName>

DESIGN ENGINEER :
Terry Lin

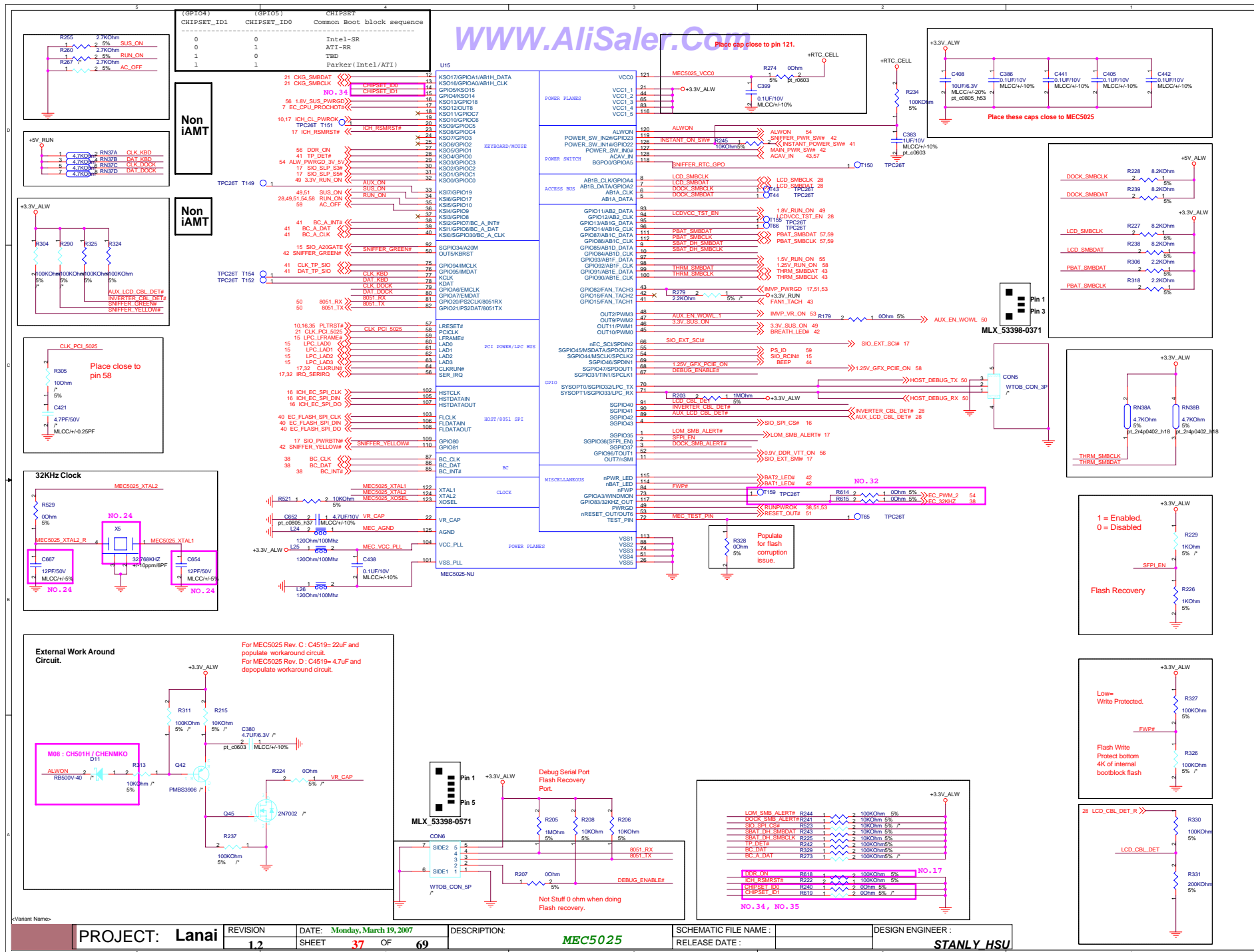


PCI-Express TX and RX direct to connector .

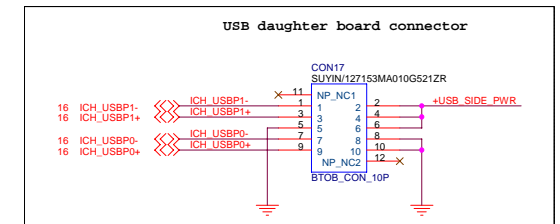
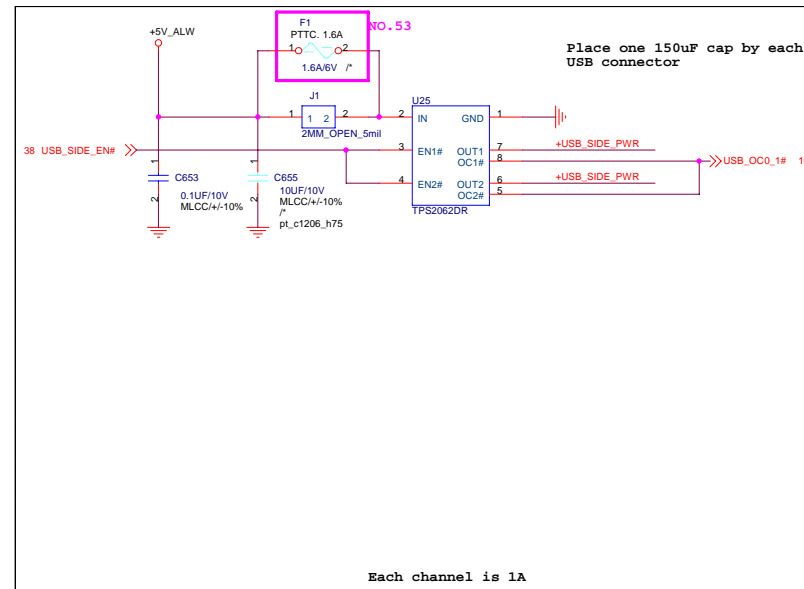




<Variant Name>		REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: MDC CONN	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
PROJECT: Lanai		1.2	SHEET 36 OF 69		RELEASE DATE :	Yihao Yeh







<Variant Name>

PROJECT: Lanai

REVISION
1.2

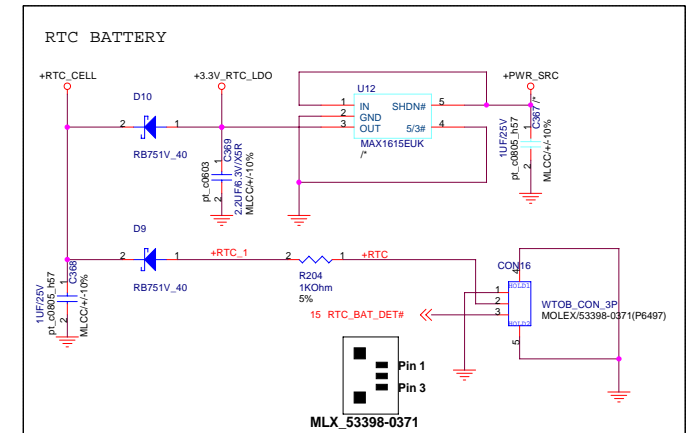
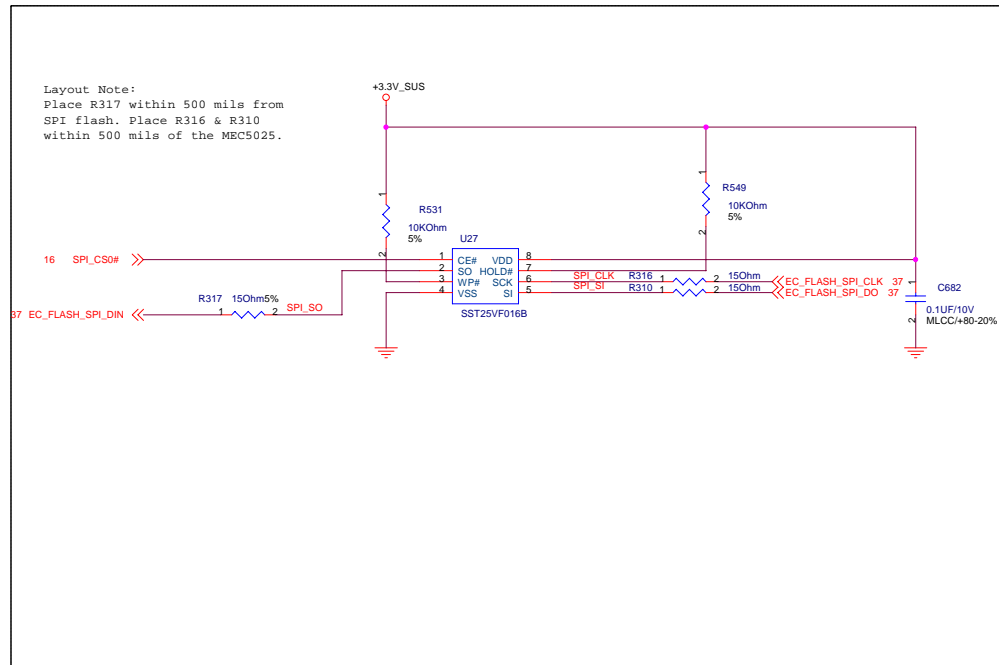
DATE: Monday, March 19, 2007
SHEET 39 OF 69

DESCRIPTION: USB PORT x 2

SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :
Terry Lin



<Variant Name>

PROJECT: Lanai

REVISION
1.2

DATE: Monday, March 19, 2007
SHEET 40 OF 69

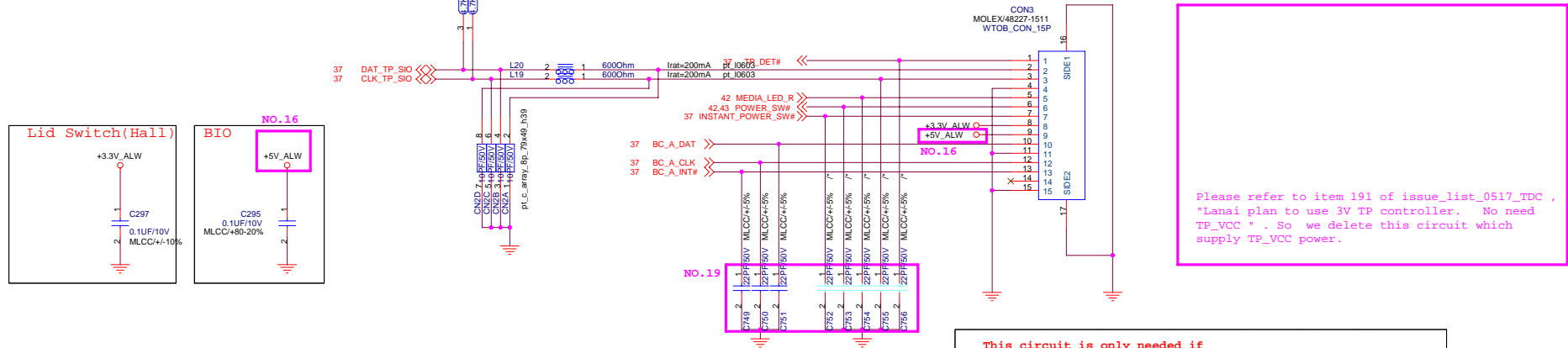
DESCRIPTION: FLASH & RTC

SCHEMATIC FILE NAME :
RELEASE DATE :

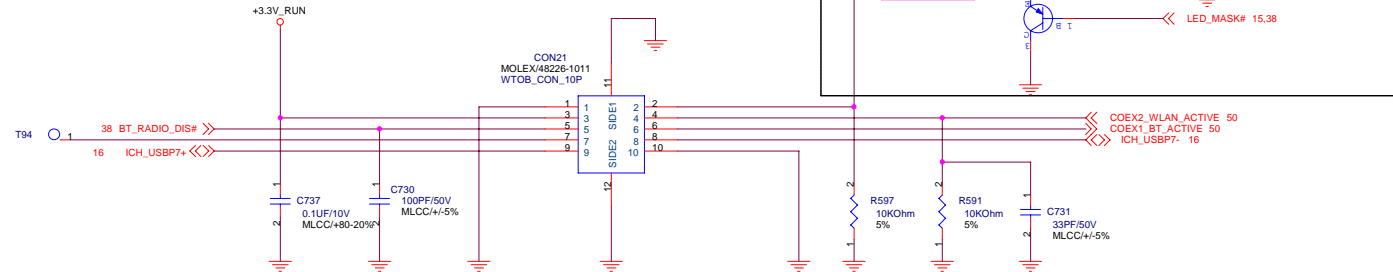
<OrgName>

DESIGN ENGINEER :
C.L. Ho

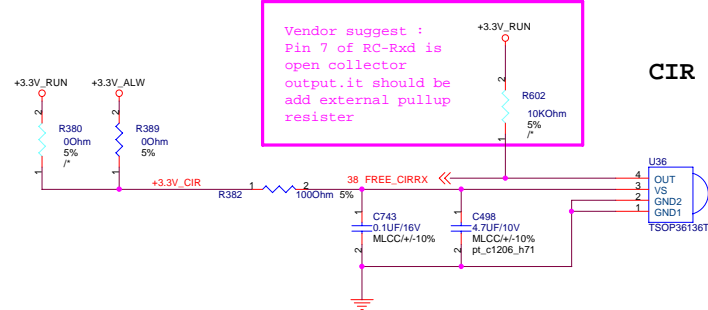
Touch Pad



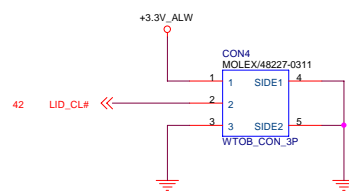
Bluetooth



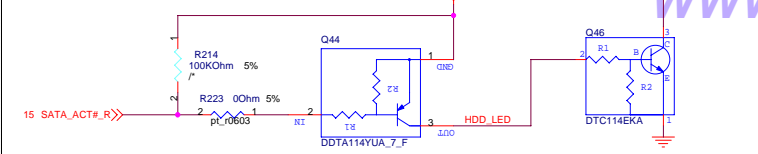
CIR



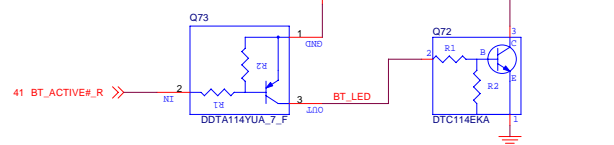
HALL SENSOR



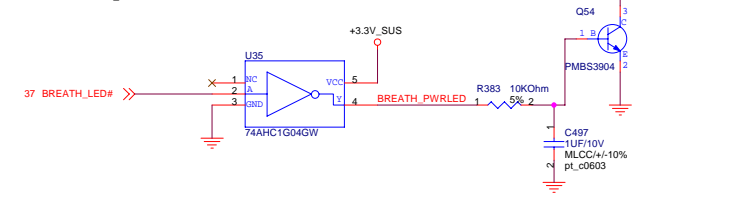
HDD activity LED



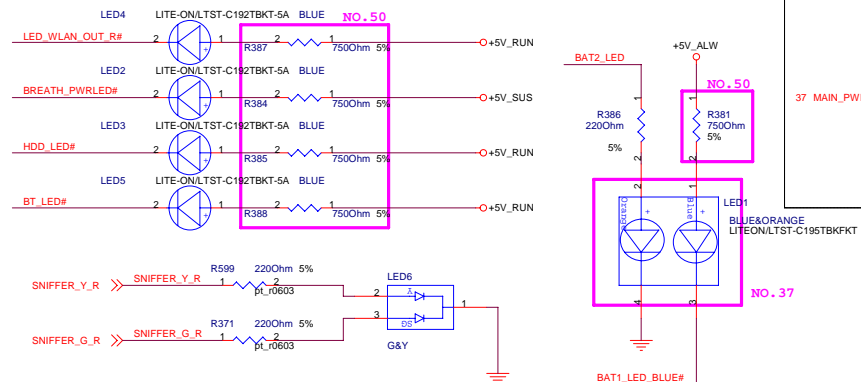
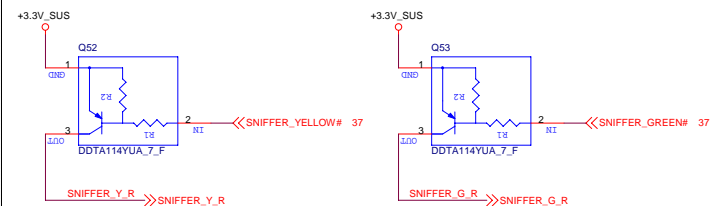
BT activity LED



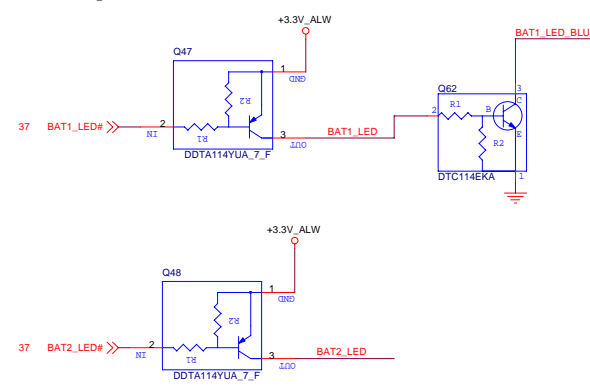
Power&Suspend



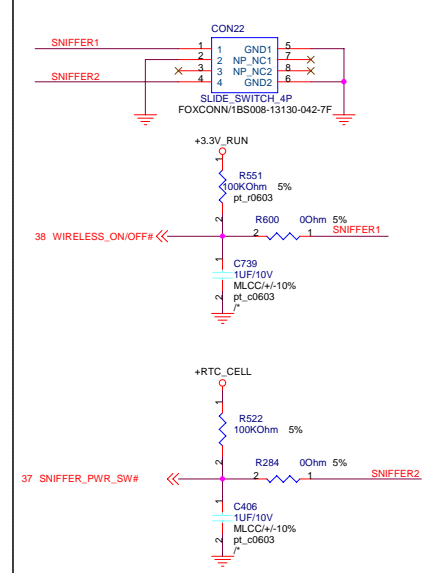
Sniffer LED driver circuit



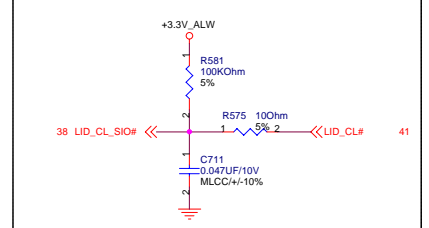
Battery status



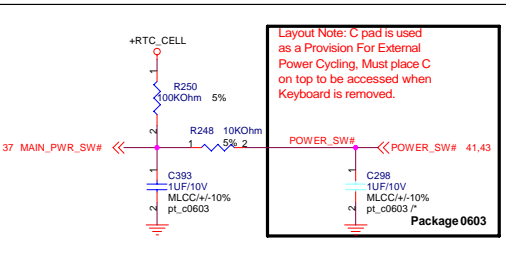
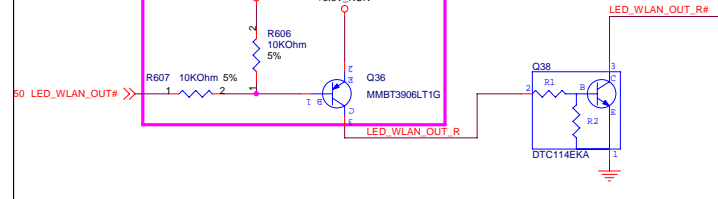
Sniffer Switch



Hall Switch

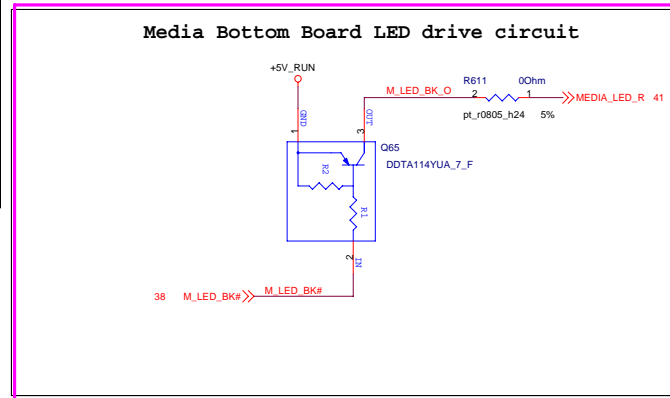


WLAN



Layout Note: C pad is used as a Provision For External Power Cycling. Must place C on top to be accessed when Keyboard is removed.

Media Bottom Board LED drive circuit



<Variant Name>

PROJECT: Lanai

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DATE: Monday, March 19, 2007
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DESCRIPTION:
SWITCH & LED

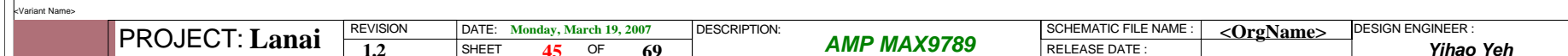
SCHEMATIC FILE NAME :
RELEASE DATE :

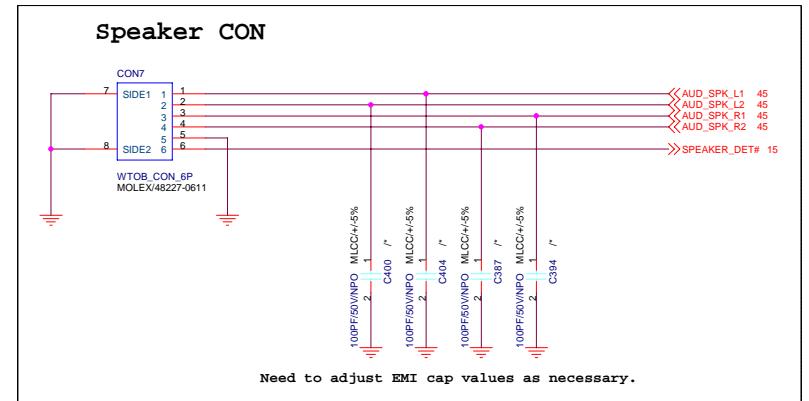
<OrgName>

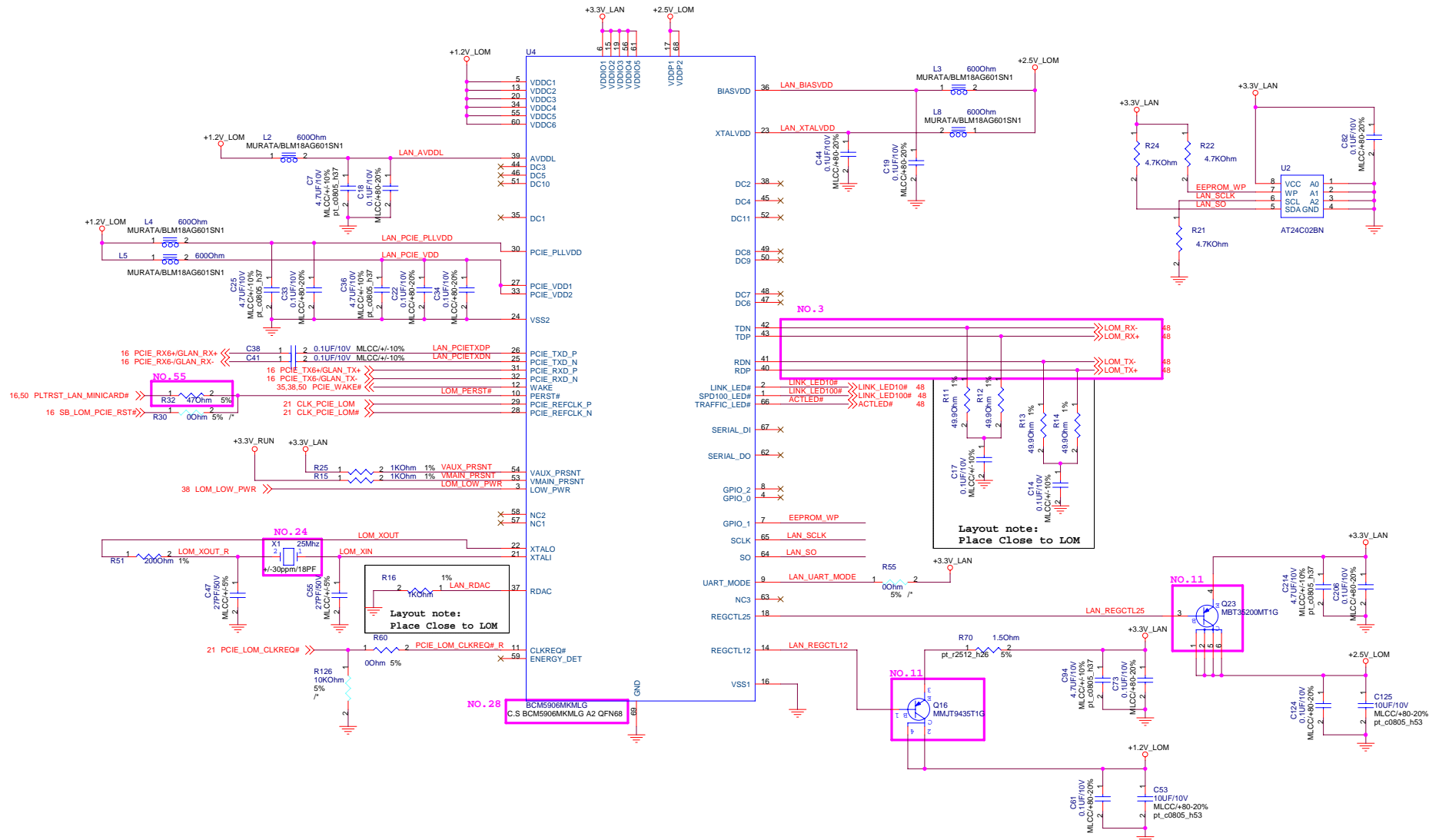
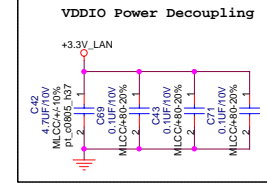
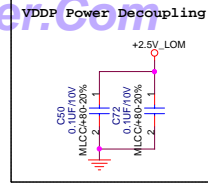
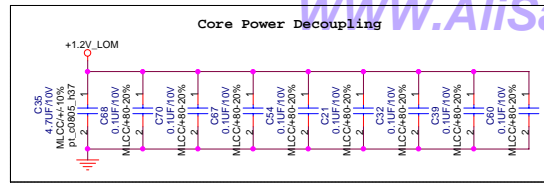
DESIGN ENGINEER :
Ivan Chou











<Variant Name>

PROJECT: Lanai

REVISION
1.2

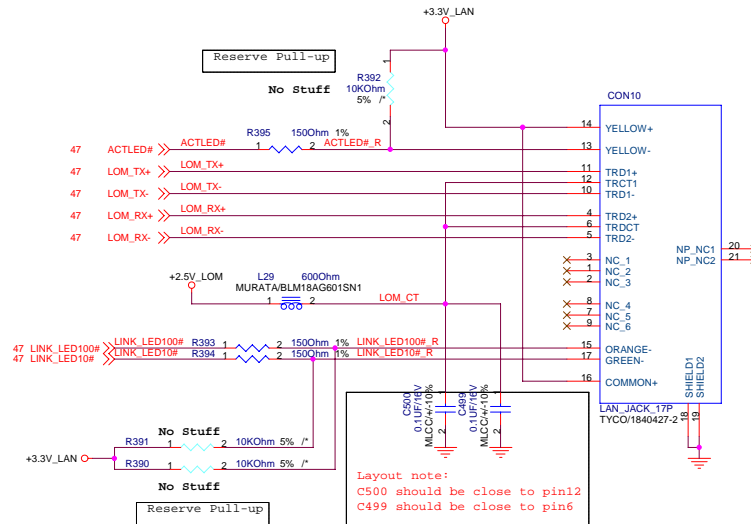
DATE: **Monday, March 19, 2007**
SHEET **47** OF **69**

DESCRIPTION:
LAN BCM5906MKMLG(QFN-68)

SCHEMATIC FILE NAME :
RELEASE DATE :

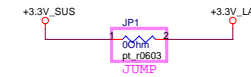
<OrgName>

DESIGN ENGINEER :
Ivan Chou



+3.3V_LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5



Per EE schematic checklist item.87: Only support wake up from S3

<Variant Name>

PROJECT: Lanai

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DATE: Monday, March 19, 2007
SHEET 48 OF 69

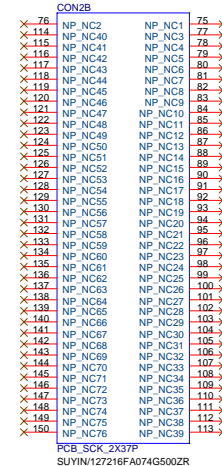
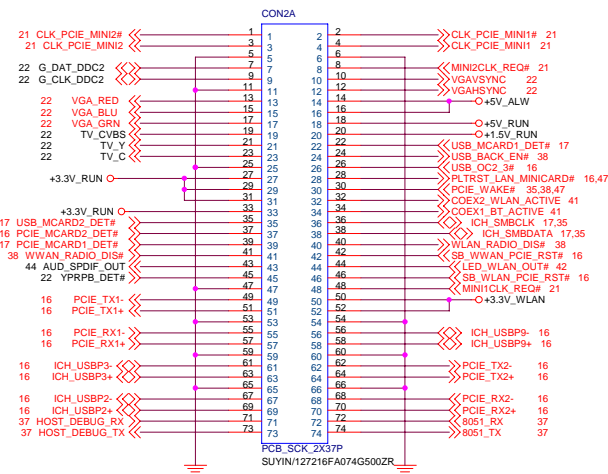
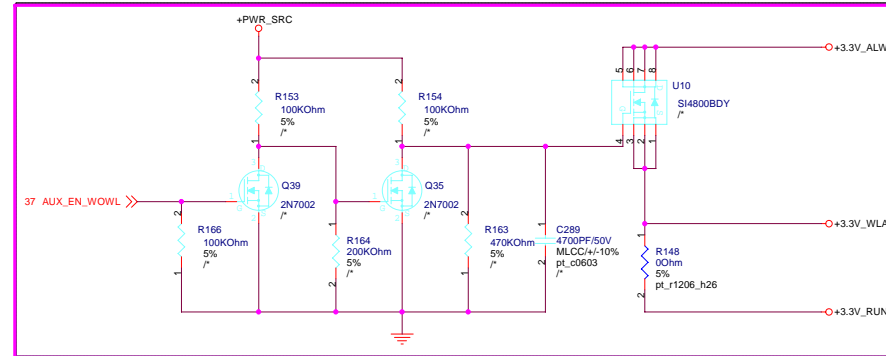
DESCRIPTION: Magnetics and RJ-45

SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :
Ivan Chou

NO. 20



<Variant Name>

PROJECT: Lanai

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DATE: Monday, March 19, 2007
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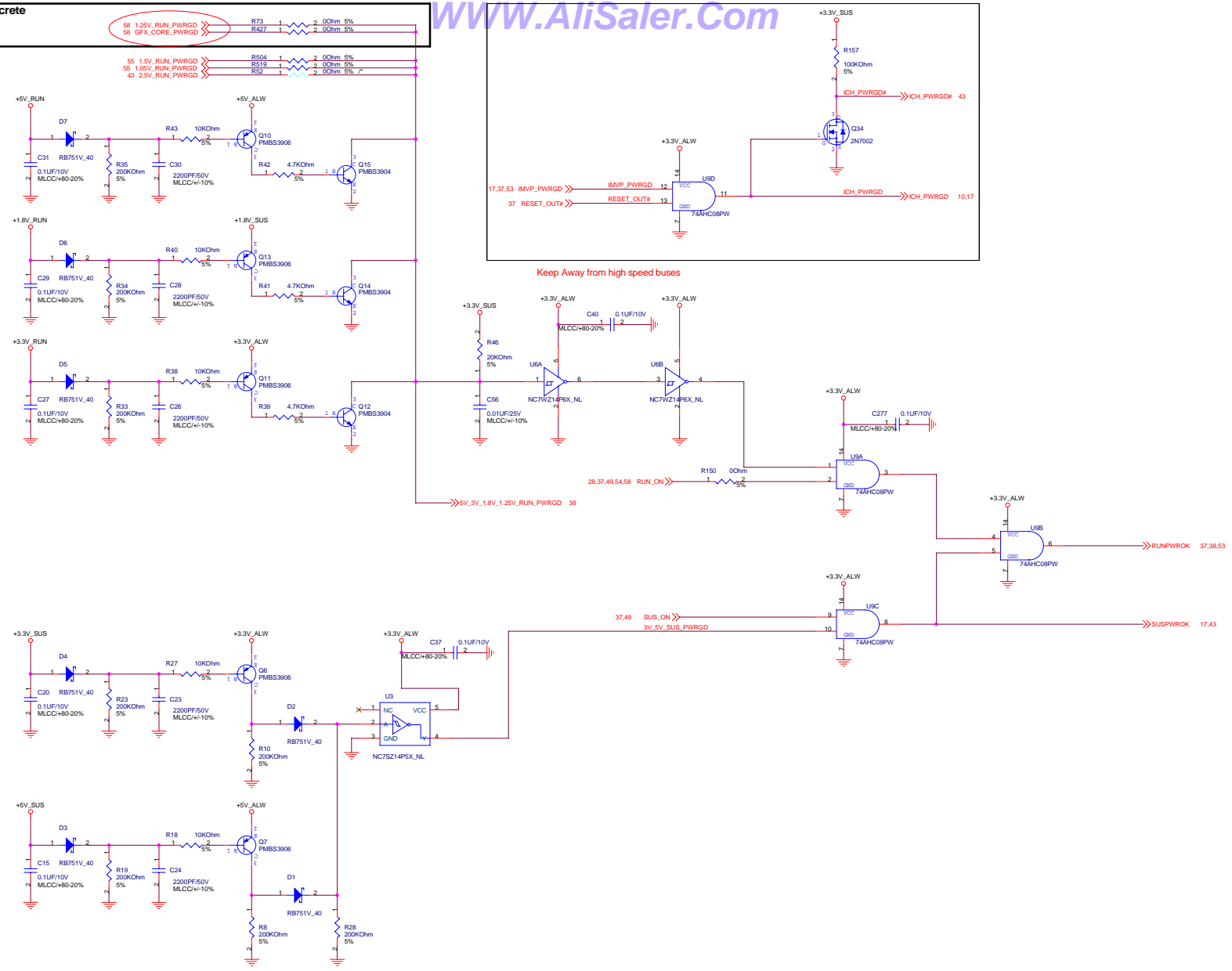
DESCRIPTION: BtoB CON

SCHEMATIC FILE NAME :
RELEASE DATE :

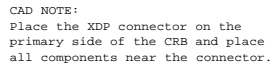
<OrgName>

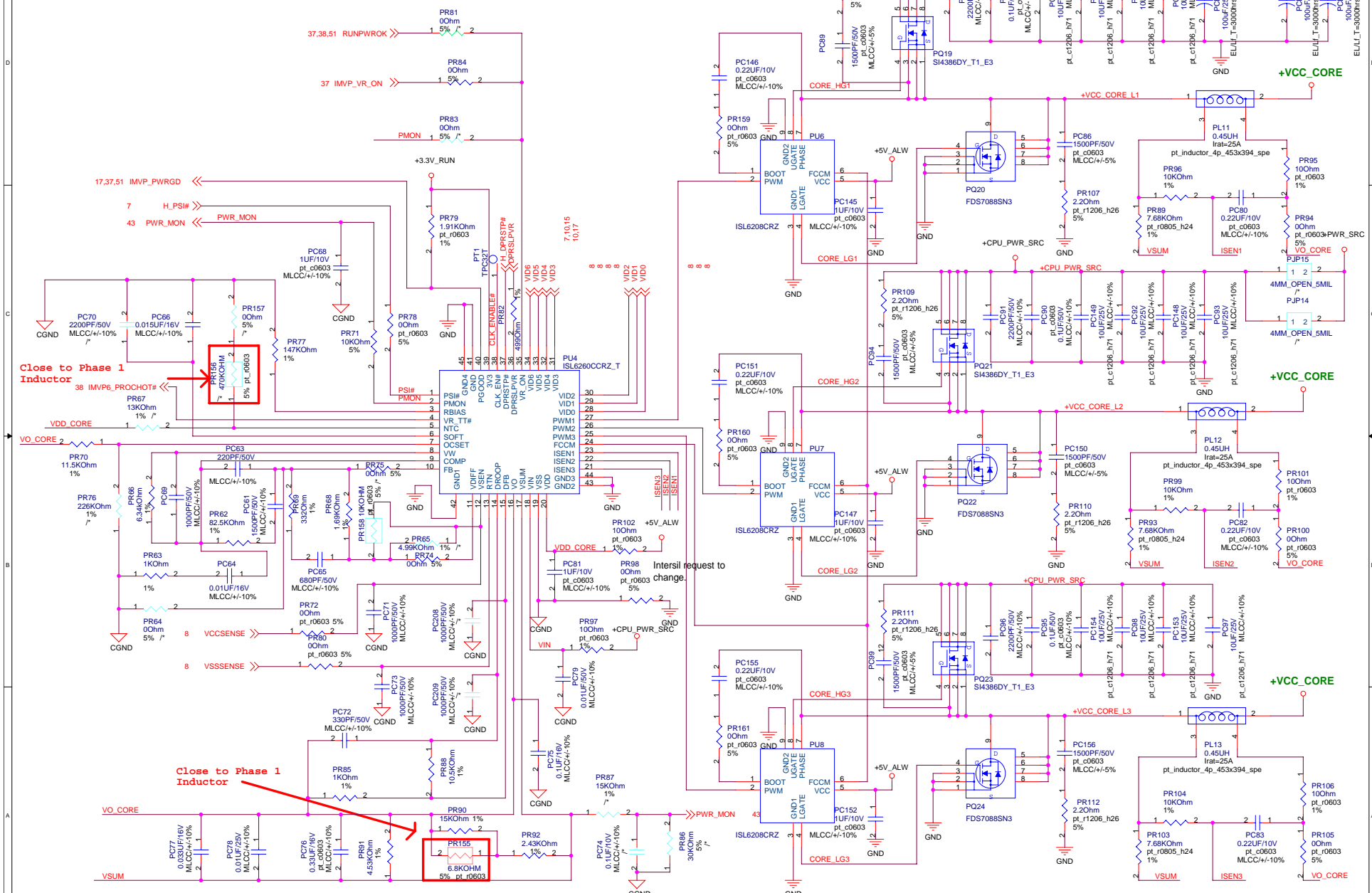
DESIGN ENGINEER :
STANLY HSU

Discrete



PROJECT: Lanai		REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Power Sequence Logic	SCHMATIC FILE NAME :	DESIGN ENGINEER :
		1.2	SHEET 51 OF 69		RELEASE DATE :	C.L. Ho





PROJECT: Lanai

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1.1

DATE: Monday, March 19, 2007

SHEET 53 OF 69

DESCRIPTION:

POWER_VCORE

SCHEMATIC FILE NAME:

<OrgName>

DESIGN ENGINEER:

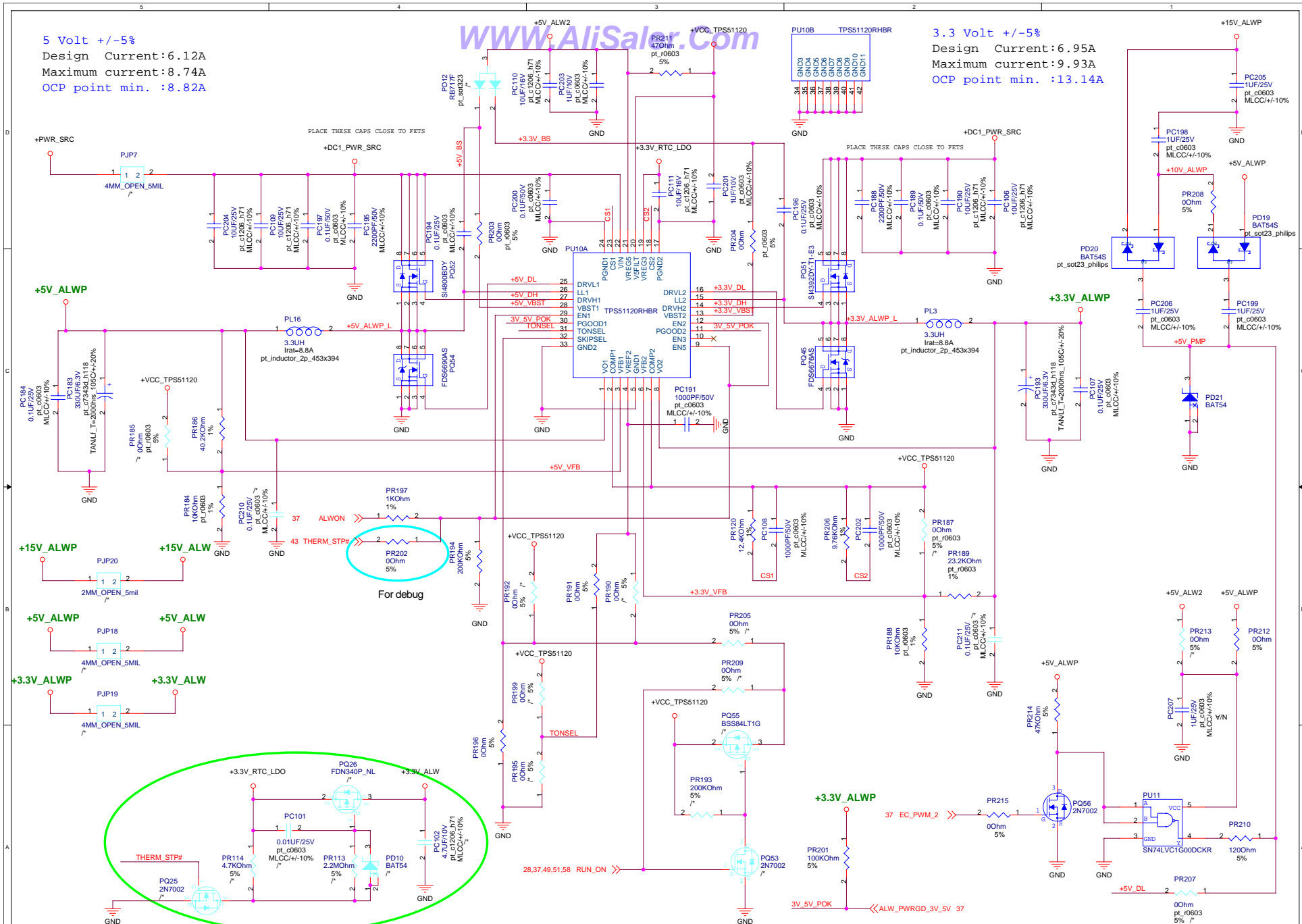
JEFF

RELEASE DATE:

5 Volt +/-5%
Design Current:6.12A
Maximum current:8.74A
OCP point min. :8.82A

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3.3 Volt +/-5%
Design Current:6.95A
Maximum current:9.93A
OCP point min. :13.14A



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DATE: Monday, March 19, 2007
SHEET 54 OF 69

DESCRIPTION:
POWER_SYSTEM5V_ALW&3.3V_ALW

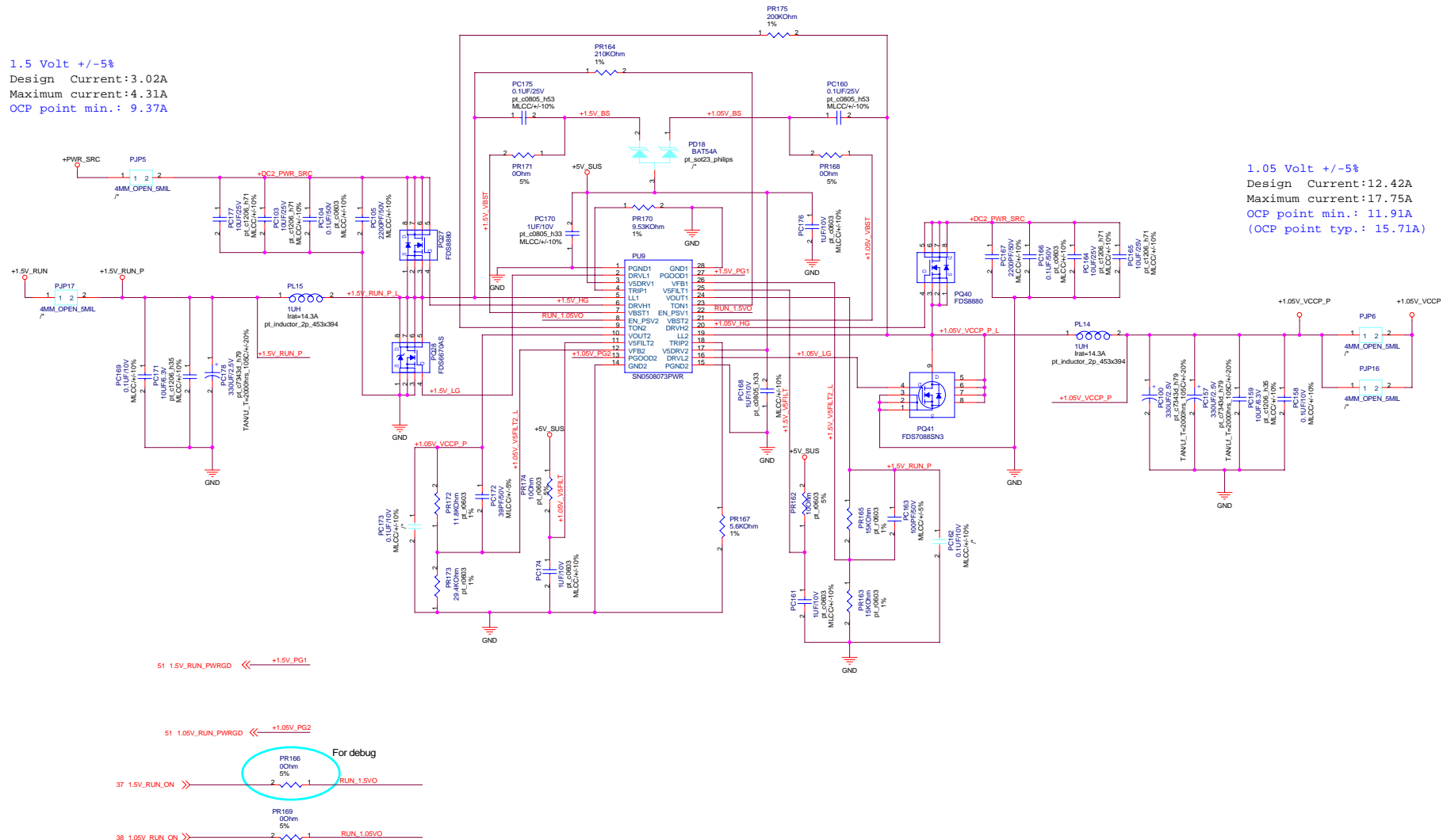
SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :
JEFF

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1.05 Volt +/-5%
Design Current:12.42A
Maximum current:17.75A
OCP point min.: 11.91A
(OCP point typ.: 15.71A)



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REVISION	DATE: Monday, March 19, 2007
1.1	SHEET 55 OF 69

DESCRIPTION:	POWER I/O 1.5VS & 1.05VS
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SCHEMATIC FILE NAME :	<OrgName>
RELEASE DATE :	

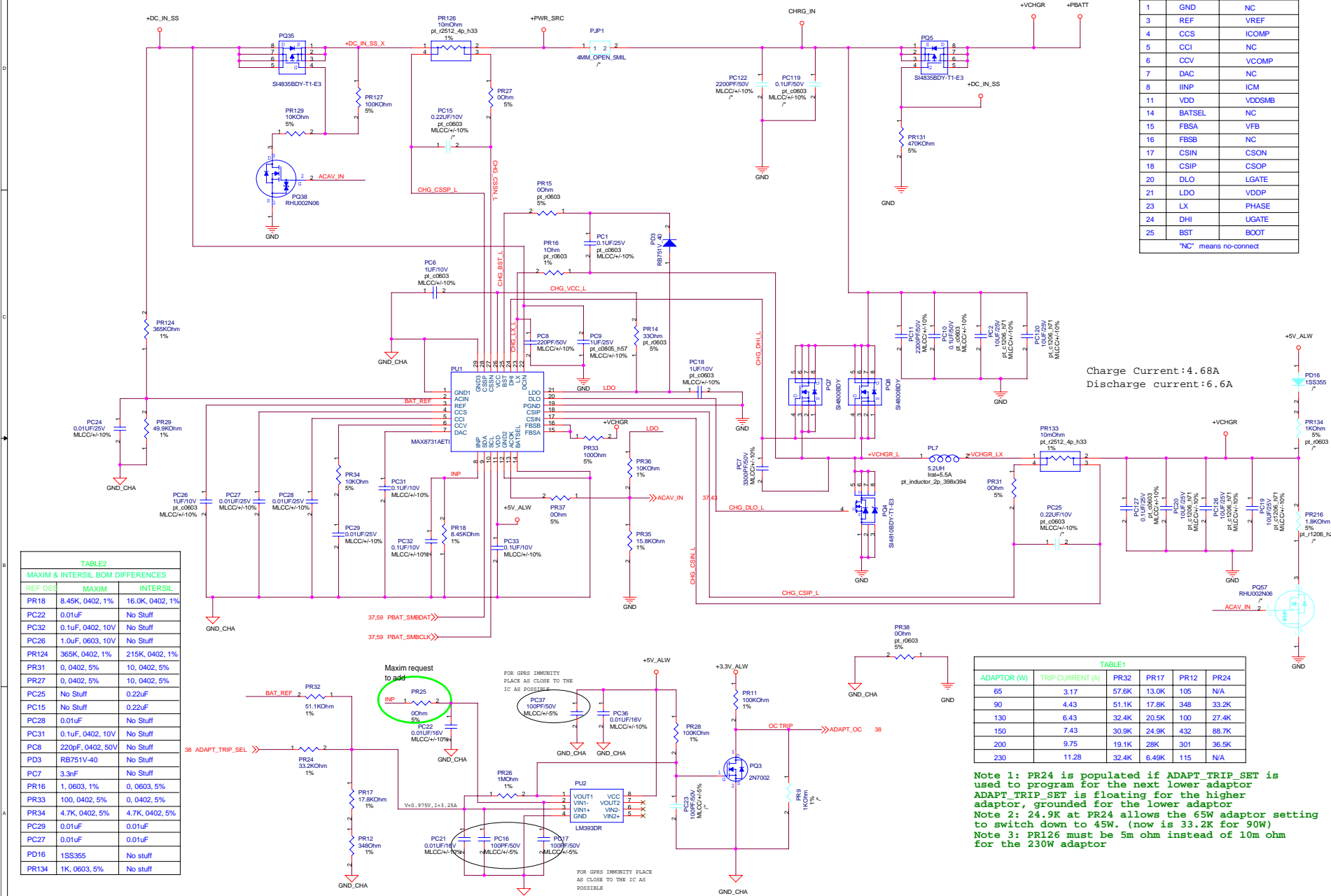
DESIGN ENGINEER :	JEFF
-------------------	-------------

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TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	OCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDD5MB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
*NC means no-connect		

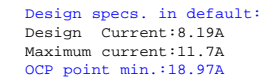


REF DES	MAXIM	INTERISIL
PR18	8.45K, 0402, 1%	16.0K, 0402, 1%
PC22	0.01uF	No Stuft
PC32	0.1uF, 0402, 10V	No Stuft
PC26	1.0uF, 0603, 10V	No Stuft
PR124	365K, 0402, 1%	215K, 0402, 1%
PR31	0, 0402, 5%	10, 0402, 5%
PR27	0, 0402, 5%	10, 0402, 5%
PC25	No Stuft	0.22uF
PC15	No Stuft	0.22uF
PC28	0.01uF	No Stuft
PC31	0.1uF, 0402, 10V	No Stuft
PC8	220pF, 0402, 50V	No Stuft
PD3	RB751V-40	No Stuft
PC7	3.3nF	No Stuft
PR16	1, 0603, 1%	0, 0603, 5%
PR33	10, 0402, 5%	0, 0402, 5%
PR34	4.7K, 0402, 5%	4.7K, 0402, 5%
PC29	0.01uF	0.01uF
PC27	0.01uF	0.01uF
PR16	1S3535	no stuf
PD31	1K, 0603, 5%	No stuf

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR32	PR17	PR12	PR24
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	148	33.2K
130	6.43	32.4K	20.5K	300	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

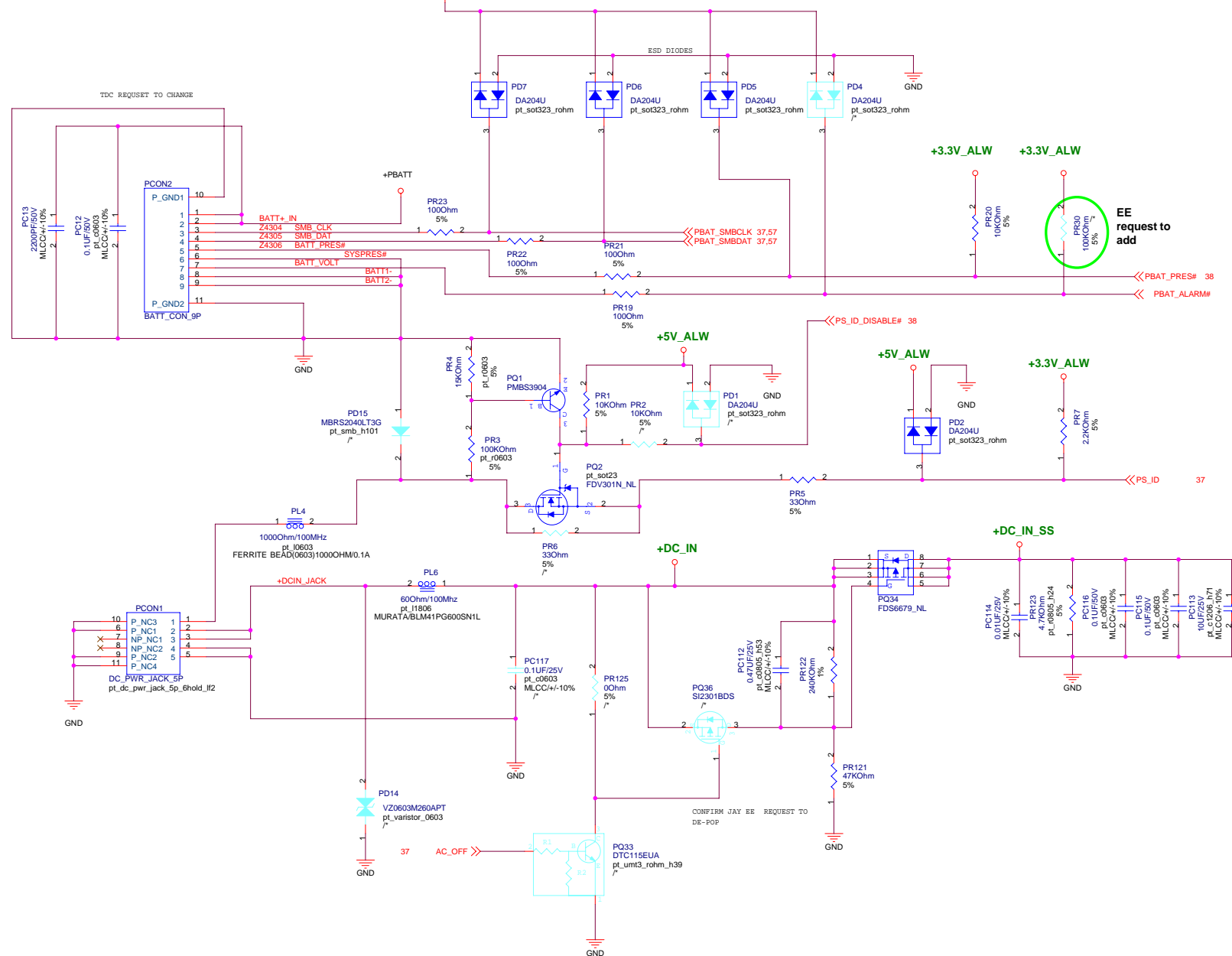
```
Note 1: PR24 is populated if ADAPT_TRIP_SET is
used in program if the next lower adaptor
ADAPT_TRIP_SET is floating for the higher
adaptor, grounded for the lower adaptor.
Note 2: 24.9K at PR24 allows the 65W adaptor setting
to switch down to 45W. (now is 33.2K for 90W)
Note 3: PR126 must be 5m ohm instead of 10m ohm
for the 230W adaptor
```

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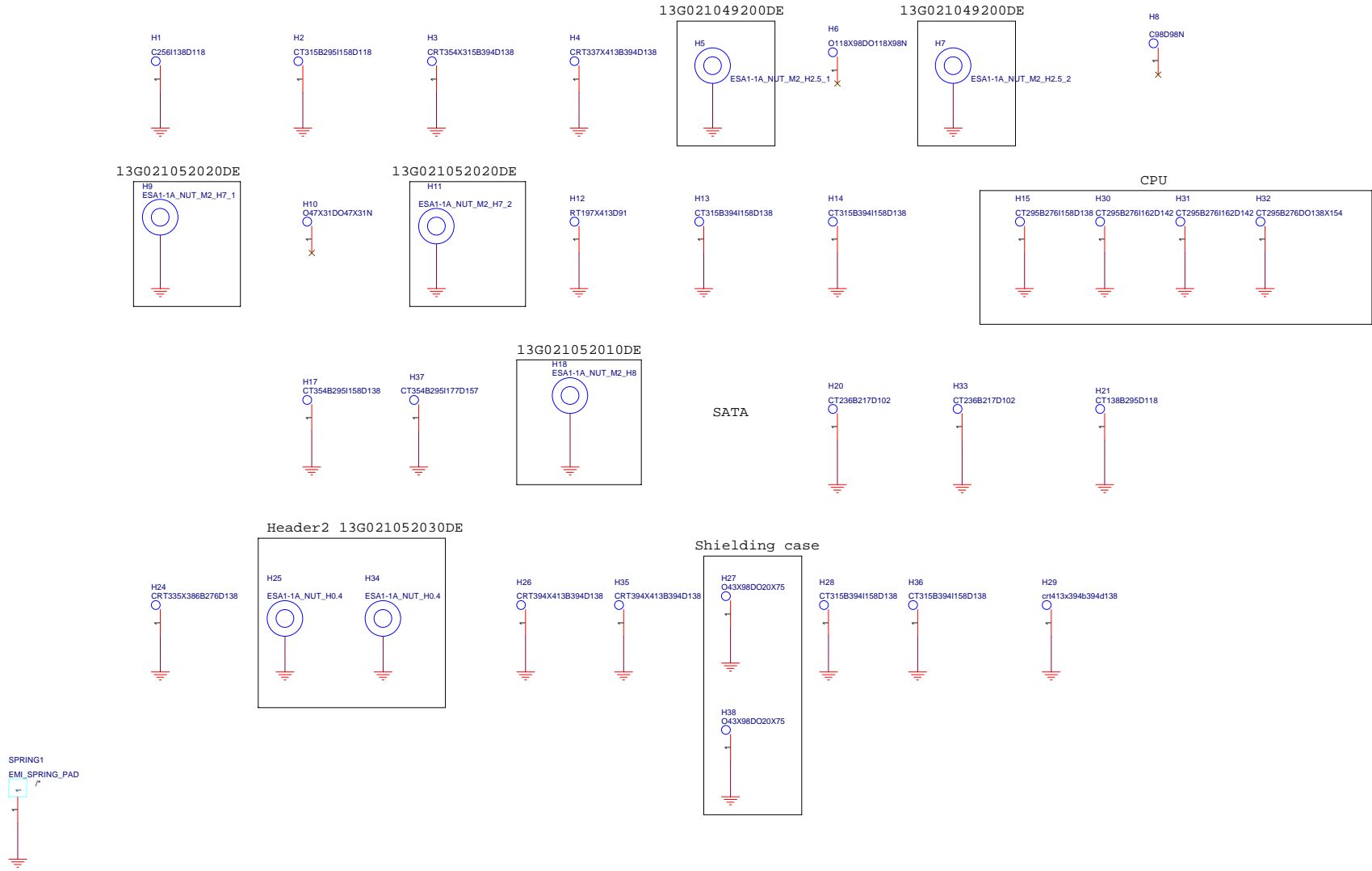
DESIGN ENGINEER :	JEFF
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DESIGN ENGINEER :	JEFF
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PM screw pad



ASUS CONFIDENTIAL

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MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

Lanai USB Board

REV :1.1(DELL: X01)

MB PCB

Part Number	Description
DAB00004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???

PCB P/N: ???

PROJECT: **Lanai**

REVISION
1.2

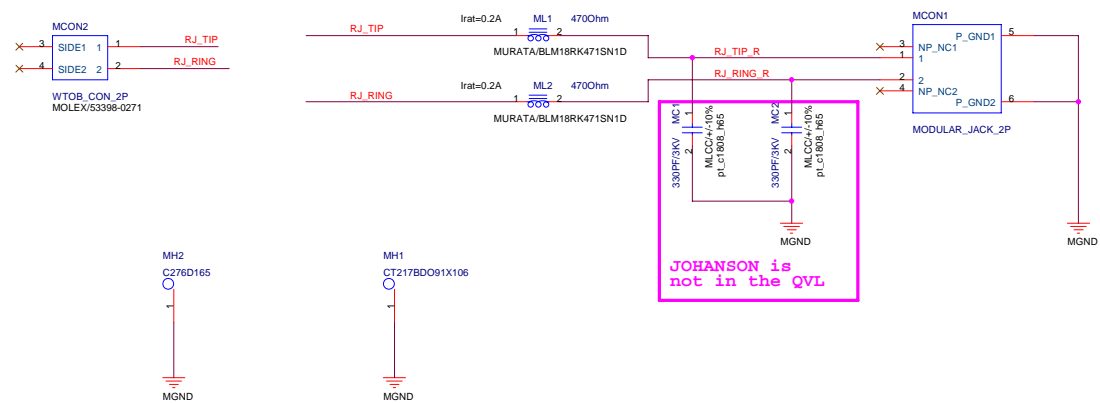
DATE: **Monday, March 19, 2007**
SHEET **65** OF **69**

DESCRIPTION: **Cover Page**

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Terry Lin

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PROJECT: Lanai

REVISION
1.2

DATE: Monday, March 19, 2007
SHEET 66 OF 69

DESCRIPTION: RJ-11 CONN

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
Stanly Hsu

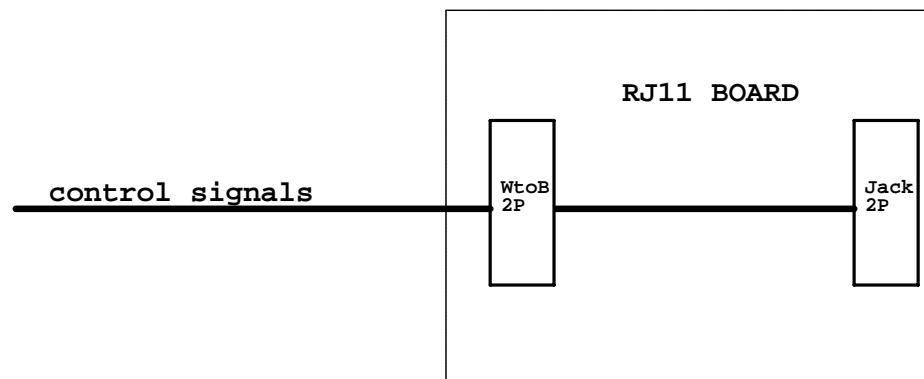
ASUS CONFIDENTIAL

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MODEL NAME : *Elsa*

Lanai Modem Board

REV :1.1(DELL: X01)



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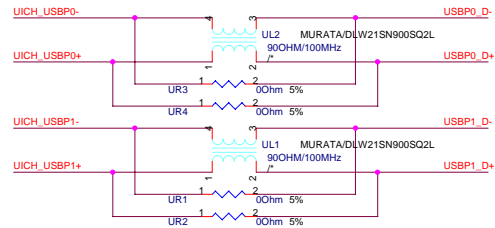
DESCRIPTION:
BLOCK DIAGRAM

SCHEMATIC FILE NAME :
RELEASE DATE :

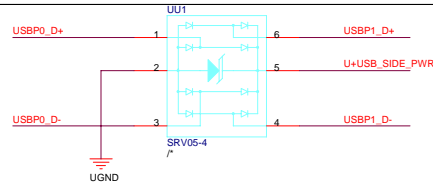
DESIGN ENGINEER :
Stanly Hsu

WWW.AliSaler.Com

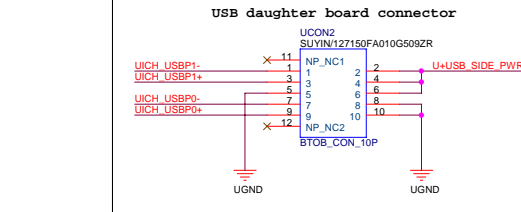
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .



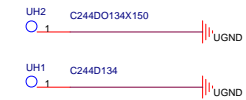
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



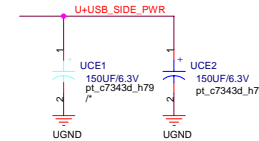
Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).



Screw hole

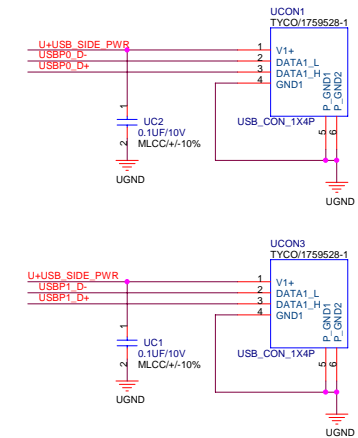


Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.



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DESCRIPTION:

USB PORT (SINGLE)

SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :

Terry Lin